

# The prospective benefits of mirroring IC package pinout

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IC packages are a vital element in the electronics interconnection hierarchy. They serve the very important function of die protection, of course, but their primary role is to transform the I/O terminals on the chip to second terminal locations that establish pin assignments at a pitch that can be more easily used by the rest of the electronics industry from design to assembly. Once pinout is established for a chip package, the locations are locked in and they are not to be changed for the life of the product in whichever package format(s) it is released. That concept is, however, being challenged by a new player now entering the packaging realm called Mirror Semiconductor<sup>[1]</sup>. The new entity is a joint effort between Liberty University and TopLine Corporation to roll out some novel intellectual property (IP) for IC packaging. The name is descriptive of the company's intention, which is to redefine I/O in a mirrored format, when it makes sense. According to the company, it can often make sense for a number of good reasons, all typically related either to package economics, their performance or both. Prospective applications for the approach include parallel data bus circuits typically found in microcontrollers, memory controllers, graphic accelerators and digital signal processing (DSP) chips, but the limits will more likely be defined by the designer.

The basic concept is simple, and it appears that it has potential to improve the efficiency of printed circuit board design in the future. This is accomplished by mixing traditionally packaged ICs with ICs having the pinout mirrored. By doing this, the developers believe it will be possible to design and build smaller circuit boards that will operate at higher speeds, require fewer circuit layers, and perhaps most important in today's competitive environment, it could also lower cost. An example will serve to make more clear how the concept might be applied.

For the last half century or so, printed circuit board designers have almost

exclusively used standard packages. There have been and still are cases where they design special packages for special needs, but such cases are exceptional. The IC devices are available with a predetermined pinout that defines which pins are signals, which are control and which are to be used for power and ground. Having such order makes the job of design easier in a sense because the library of components is stable. The board layout process is driven by a schematic that defines which components are to be connected to which other components and at which pin locations. In the ideal world, all components could be located so that all of the connections were optimal, but the chances of that ever

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happening reside somewhere between slim and none. Instead, computer automated design tools are used to make sense of the interconnection assignment and define appropriate or best fit routes for the copper traces that serve as electrical and electronic circuits. When the software detects an 'in plane' intersection of traces, it normally solves the problem by routing one signal over or under the other by the addition of layers and the tactical use of plated vias. Unfortunately with today's higher speeds, the addition of layers and vias normally brings with it a lot of problems relative to signal integrity due to added noise, stray capacitances and inability to balance characteristic impedance. To solve this, the developers suggest judicious intermixing of standard

and mirror pinout devices. In certain applications the benefit seems very clear; for example it offers the designer the opportunity, in some cases, to get the benefit of stacking devices without stacking but instead by simply assembling the mirrored component on the side opposite the standard device. In such a case the signal is radically shortened.

The idea appears to have some merit, but it may take a short while for the thinking to catch on. The creation of a second part number for the same device increases logistical and inventory challenges, but they don't appear to be overwhelming on first consideration. It does offer potential to reduce design complexity, but it also increases to some degree the assembly. In the end analysis, it will be the benefits that will define the success of the technology. Certainly the promise of lower cost combined with higher performance seem compelling enough to warrant further investigation.

[1] [www.mirrorsemi.com](http://www.mirrorsemi.com)

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