



Example 1: Ball Grid Array (BGA) and Quad Flat Pack (QFP) Design.

Traditional Design: At Liberty University, an 8-layer PWB was designed using two traditional BGA and two traditional high pin count QFP components, placing one of each component on each side of the PWB. This well designed PWB required hundreds of common connections.

Redesign with Mirrored Pinout: By revising the design to mate the traditional components on one side of the PWB with Mirrored Pinout components on the other side, we were able to complete the design with only a 4-layer PWB.

Result: Reduction in the PWB design from 8-layers to 4-layers. Significant improvements in overall circuit performance with significant cost reductions were achieved.

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Example 2: Simple 3-pin Transistor Design.

Traditional Design: Connection of 3-pin transistors in a communications circuit.

Redesign with Mirrored Pinout: Mate the traditional transistor with Mirrored Pinout transistor to simplify connections.

Result: Removing two vias per differential circuit.

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Example 3: Four QFP, 2-Layer Design

Traditional Design: Four 100-pin traditional QFP mounted all on one side of a 2-layer PWB with 375 vias and total copper trace length of 487 inches.

Redesign with Mirrored Pinout: Inter mix two Mirrored Pinout QFP with two traditional QFP (all on one side of a 2-layer PWB, to keep apples to apples comparison).

Result: The redesigned PWB required only 188 vias with a total copier trace length of 432 inches. While the length of the circuit tracing was not significantly lowered, the revised design completely eliminated errors during the autorouting standard default setup.

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Additional design examples available on request.

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