Joe Fjelstad

Bottom terminated component (BTC) technology follows growing market demand for lower profile packaging

IC packaging is an area of technology that seems to offer an endless stream of innovation for the electronic product or system designer. One area of increasing interest in recent years is the family of bottom-leaded components whose representatives include the increasingly common quad flat no-lead (QFN) devices and land grid arrays (LGA). These devices are especially attractive for cost and performance reasons, and for the low profile they offer in an electronic assembly, but they also represent a significant challenge to the assembly process due to their lack of stand-off height. Presently, the IPC is in the process of developing a standard to address these issues and provide guidance going forward. The document IPC-7093, titled "Design and Assembly Process Implementation for Bottom Termination SMT Components," is in working draft form and is expected to be out for review later this year or early next.

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Relative to the referenced innovations in the BTC packaging arena, a package offering that is getting increased attention in recent months is being developed and marketed by Mirror Semiconductor in Irvine, CA (www.mirrorsemi.com). The company has been developing a family of open cavity QFN packages for the semiconductor market, and they are finding demand from a number of different areas.

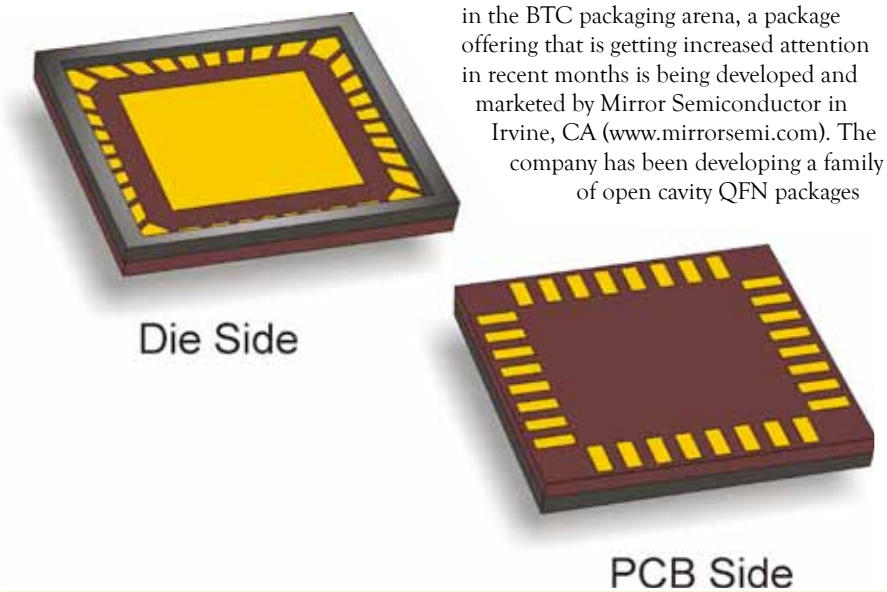

Figure 1. Bottom terminal components such as QFNs and LGAs are among the most rapidly growing package types in terms of use. Above are shown opposing side views of an air cavity bottom terminated package concept being produced and offered by Mirror Semiconductor in Irvine, CA .

While the structures in finished form appear to be QFN type, they are actually different in their construction, which makes them stand apart from their "siblings." That is, instead of using copper lead frames, which would be a difficult fit for such applications, Mirror Semiconductor is using 200 µm (8 mil) thick rigid substrates. Both Mitsubishi BT and Rogers RO4003C substrates are being used at present for standard and high frequency applications, and the company indicates that other substrate materials will be considered in the future. The open cavity QFN (see Figure 1) is a wire bonded structure and to assure that good wire bonding is achieved, the cavity side of the substrate is plated with ~1.25 µm (~50 microinches) of wire-bondable gold.

Presently the cavity is formed by dispensing in a process similar to that used for chip-on-board applications in the creation of dams for encapsulant. This is very simple and easily modified as there are no physical parts to assemble or tooling required, but it does have some limitations when it comes to use of a lid because the rim of the cavity is rounded rather than

flat, due to the nature of the resin used and the dispensing process. Still, where the IC is to be over molded, this concern is obviated. However the company is nevertheless looking at alternative methods which could fully ameliorate the issue.

Interconnection from side to side on the package is accomplished using filled via in pad technology to connect from top side to bottom side. The finished contact on the SMT side is all metal and flat, which eliminates normal concerns about void formation in via in pad designs. The surface finish for the surface mount lands is of the electroless nickel immersion gold (ENIG) type.

Reviewing the areas of interest is interesting in its own right. Following are a few of the applications that are looking at open cavity technology in QFN format. One that is seemingly well suited to the technology is that of test and prototype where typically the demand is for small quantities (e.g. less than 500 pieces) The package structure is highly amenable to getting a die into a package and then being able to exercise and even perform diagnostics because before the lid is applied, the die can still be seen and accessed if desired.

Other areas of interest for the technology include packaging MEMS devices, RF and microwave and optical/photonic sensors such as UV EPROMs, CCDs or lasers. Given that many MEMS device application require access to the outside world the high level of interest reported seems sensible.

Mirror Semiconductor president Martin Hart has indicated that the company is building a world wide network of assembly houses to provide customers with QFN open cavity packaging and assembly in multiple locations around the globe.

In summary, the family of BTC components continues to evolve and grow to meet the cost and performance needs of electronic product designers and developers. These planar lead devices are likely to see much increased use in the coming years as interconnection technology itself continues to grow and evolve. One example of note, and pointed out in earlier columns, is as a packaging solution of first choice for Occam Process assemblies where solder is replaced by copper plated interconnections. Still solder will likely have a long run ahead and having standards in place such as the IPC 7093 will definitely serve an important need by providing a focal point for understanding these important package types.

Verdant Electronics founder and president Joseph (Joe) Fjelstad has more than 35 years of international experience in electronic interconnection and packaging technology in a variety of capacities from chemist to process engineer and from international consultant to CEO. Mr. Fjelstad is also a well known author writing on the subject of electronic interconnection technologies. Prior to founding Verdant, Mr. Fjelstad co-founded SiliconPipe a leader in the development of high speed interconnection technologies. He was also formerly with Tessera Technologies, a global leader in chip-scale packaging, where he was appointed to the first corporate fellowship for his innovations.