CHIP PACKAGING 2.0 – USER DEFINABLE CHIP PINOUT PACKAGING FOR OPTIMIZED PC BOARD DESIGN

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ABSTRACT
System designers have an ongoing need to optimize board-level designs. The cost to spin new chips from scratch is prohibitive in today's business environment. Legacy chips are routinely thrown "over the wall" to board designers, often years after the chips were designed. In the current world, legacy chipmakers have limited interest to talk with board designers. Board designers are constrained from developing fully optimal boards in the current so-called "Chip Packaging 1.0" environment and there is a clear need to change.

In the proposed new "***Chip Packaging 2.0***" environment, board designers start with off-the-shelf legacy die (wafer) and use suitable EDA software to re-map the chip's pinout (without altering the performance of the silicon) while simultaneously optimizing the board design. The EDA software would create a bonding schedule for delivery via the internet or by conventional means to wirebonding machines for assembly.

This paper poses the question *what if* board designers were empowered to re-map legacy chip package pinouts, in order to design optimum boards in a Chip Packaging 2.0 world?

Prevailing conventional wisdom in today's Chip Packaging 1.0 world presumes that only the chip design team is qualified to define IC package pinouts. That argument is compelling, since the chip design team is most familiar with the silicon chip, and therefore most qualified to determine the packaging and pinout. Since no communications channel exists between the Chip Packaging 1.0 silicon design team and the board designer, boards are chronically constrained from being fully optimized.

For purpose of this paper, an "optimized" or "optimal" board shall be defined as being the smallest in size, with shortest copper routing, fewest inner-layers operating at the highest performance, and potentially having the quickest development time to market.

Keywords: chip packaging 2.0, mirrored pinout, reversed pinout, UDPo

INTRODUCTION
Chip Packaging 1.0 is what the industry fundamentally practices today. The chip design team defines the package and pinouts. No communication channel exists between the chip design team and the board design team. Packaged chips are simply tossed over-the-wall to board designers who are highly constrained in today's Chip Packaging 1.0 environment (Figure 1). The IC package pinouts are documented in the chipmaker's datasheets. Board designers have no ability to change any aspect of the IC package or to re-map the pinout in the current Chip Packaging 1.0 world. Board designers thus have one hand tied behind their back from the very beginning of the board design cycle.

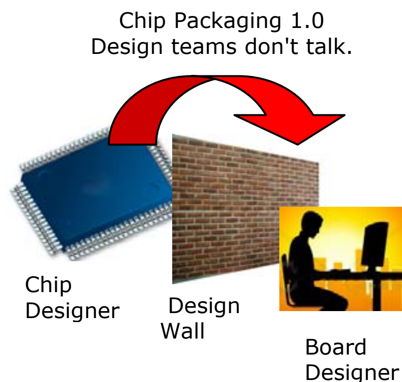


Figure 1. Chip design team defines the package pinout without collaboration with board designer.

In spite of these issues, the old style Chip Packaging 1.0 protocol may never go away entirely. However, advantages attained in the proposed Chip Packaging 2.0 environment are compelling and should be examined.

In Chip Packaging 2.0, board designers use EDA software to iterate IC package pinouts of legacy die (wafers) while simultaneously optimizing the board's routing (Figure 2.)

Such semiconductor packaging is referred to as "User Definable Pinout" (**UDPo**).

Proposed Chip Packaging 2.0 protocol.

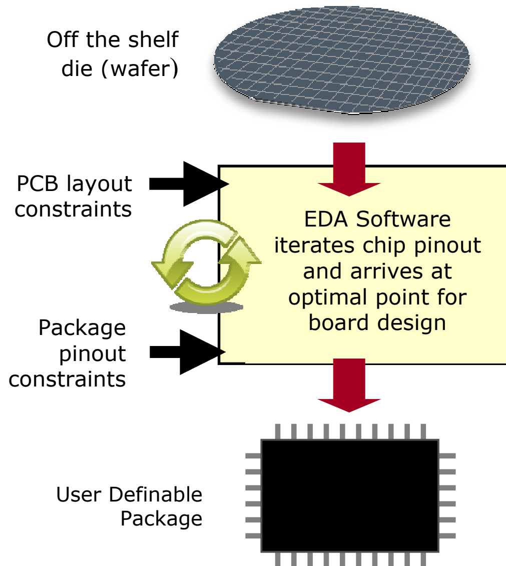


Figure 2. EDA software iterates UDPo - User Definable Package pinouts until board layout is optimized.

In the proposed Chip Packaging 2.0 environment, board designers are empowered to re-map package pinouts of legacy chips using EDA software without altering the performance of the silicon. Typically during the circuit board's initial design process, the board designer makes a series of tradeoffs between electrical, thermal and mechanical needs. Once component locations are established, the circuit schematic is loaded and autorouting of the board commences. The iteration begins by benchmarking the initials results achieved with "standard pinout" packages. Next, the EDA software begins the pinout iteration process. Pairs of pinouts on selected IC packages are iterated while board routing is observed. During the iterative process, improvement is observed as copper routing is shortened, board size is reduced and/or fewer inner layers are required. Circuit speed improves roughly one nanosecond in a theoretical lossless substrate for each 6-inch (150mm) reduction of dual copper path (signal plus ground) according to the speed of light formula [1].

Typically the pinout of one chip at a time is optimized, then cycled to the next chip until the total circuit board is optimized to the satisfaction of the board designer. Once the chip pinouts are optimized, the EDA software will output a bonding schedule (net list) for input into wire-bonding machines.

Chip packages are bonded using insulated bonding wire, to prevent shorting inside the IC package.

Another way to design optimum boards is by mating "standard" integrated circuits with mirrored pinout packages. The circuit shown in Figure 3 is built on a single layer board, without the use of vias.

The device on the right is standard IC. The device on the left contains the same silicon die, but the package pinouts are "mirrored" (reversed).

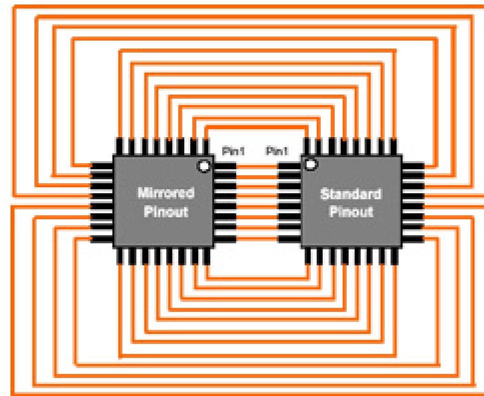


Figure 3. Single layer routing achieved when mirrored pinout device is bussed with standard IC.

Figure 4 is a circuit built on a two layer (double sided) board. The top device (U1) is a standard pinout package. A mirrored pinout chip (U2) is mounted on the bottom of the board and connected by plated vias. The copper routing from U1 to U2 is approximate the same length as the thickness of the board.

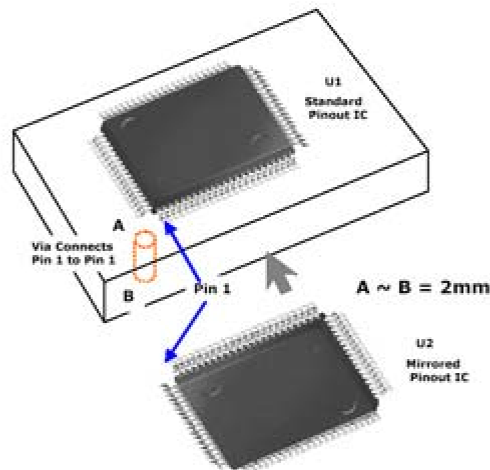


Figure 4. Mirrored pinout U2 is bussed to standard device U1. Routing length is thickness of the board.

It is important to recognize that bussing a “standard” device to a “mirrored pinout” device is completely different from “mirroring” similar devices on the top and bottom side of the board.

In figure 5, pins on the top “standard pinout” package (starting with pin 1) match and align with corresponding pins on the bottom mounted “mirrored pinout” device. Pin-to-pin alignment continues to occur even when the “mirrored pinout” package is mounted on the topside and “standard pinout” package is mounted on bottom of the board.

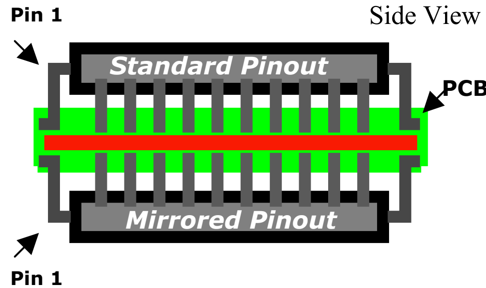


Figure 5. True Pin-to-pin alignment of “mirrored pinout” device with standard pinout device.

In Figure 6 a pair of “standard pinout” devices are “mirrored”, one over the other the board. Note that pin 1 of the top component does not align with pin 1 of the bottom component.

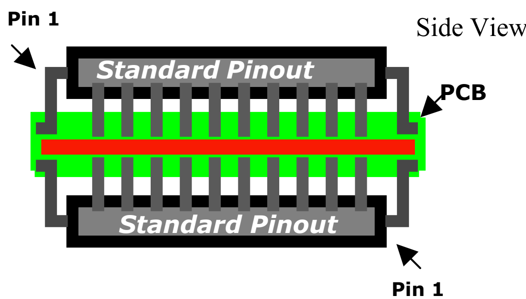


Figure 6. Pins misalign when “mirroring” two similar devices. Note location of pin 1.

Figure 7a,b shows the top view of a “standard pinout” and “mirrored pinout” device. The pin numbering of “standard pinout” devices is counterclockwise. The pin number of “mirrored pinout” devices is clockwise. Figure 7c illustrates that when a “mirrored pinout” device is flipped and mounted on the bottom side of the board, the pin numbering exactly matches and aligns the “standard pinout” device.

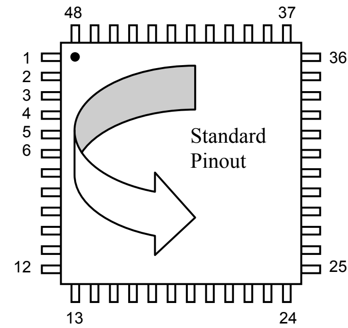


Figure 7a. Counterclockwise pin numbering of “standard pinout” device.

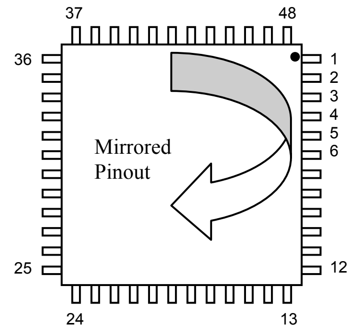


Figure 7b. Clockwise pin numbering of “mirrored pinout” device.

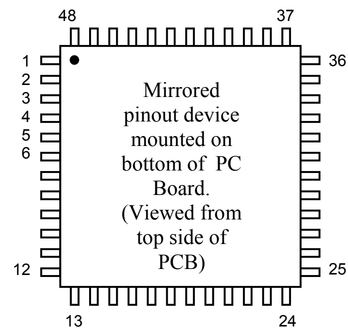


Figure 7c. Pins of a bottom mounted “mirrored pinout” exactly match the “standard pinout” when viewed from the top side of the board.

BACKGROUND

Early initiatives to optimize PC boards were performed by bending and contorting the pins of Dual in-Line (D.I.P.) packages using plated throughhole technology (Figures 8). The inventor claimed that such configuration doubled the memory storage capacity of the PC board module [2].

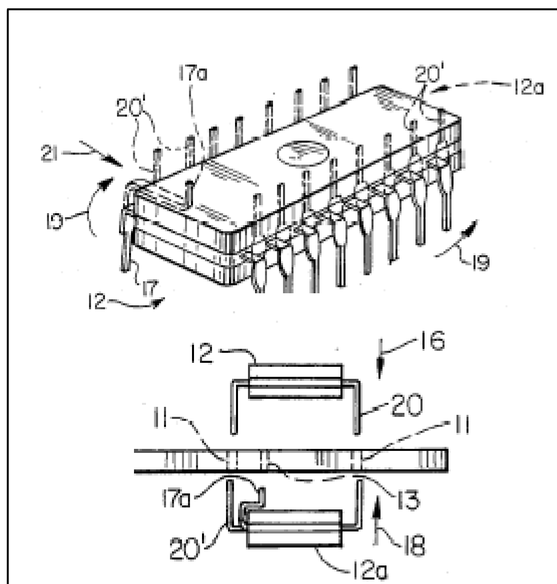


Figure 8. Early attempt to create high-density memory modules by bending the leads on DIP packages.

The bottom device in Figure 9 shows an example of a gull-wing mirrored pinout SOIC invented in the 1980s. Thinner TSOP mirrored pinout memory packages later became readily available in the 1990s. The lead frame is reverse formed after molding to create the "mirrored pinout" package. By mating "standard pinout" devices on one side of the board with "mirrored pinout" devices on the other side of the board, it is possible to optimize the routing of memory modules [3].

Figure 9. Bottom device gull wing leads are "reversed" formed in the opposite direction during trim and form.

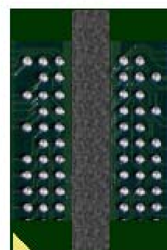
In the late 1990s, memory device makers introduced Ball Grid Array (FBGA) and CSP packages with "reversed pinouts" Figure 10a is an example of a standard pinout RAMBUS® DRAM. Figure 10b depicts the "mirrored pinout" version [4].

12	GND		VDD				VDD		GND
11									
10	DQA7	DQA4	CFM	CFMN	RQ5	RQ3	DQB0	DQB4	DQB7
9	GND	VDD	GND	GNDa	VDD	GND	VDD	VDD	GND
8	CMD	DQA5	DQA2	VDDa	RQ6	RQ2	DQB1	DQB5	SIO1
7									
6									
5	SCK	DQA6	DQA1	VREF	RQ7	RQ1	DQB2	DQB6	SIO0
4	VCMOS	GND	VDD	GND	GND	VDD	GND	GND	VCMOS
3	DQA8	DQA3	DQA0	CTMN	CTM	RQ4	RQ4	DQB3	DQB8
2									
1	GND		VDD				VDD		GND
	A	B	C	D	E	F	G	H	J

Figure 10a is "standard pinout" DRAM BGA.

12	GND		VDD				VDD		GND
11									
10	DQA8	DQA3	DQA0	CTMN	CTM	RQ4	RQ4	DQB3	DQB8
9	VCMOS	GND	VDD	GND	GND	VDD	GND	GND	VCMOS
8	SCK	DQA6	DQA1	VREF	RQ7	RQ1	DQB2	DQB6	SIO0
7									
6									
5	CMD	DQA5	DQA2	VDDa	RQ6	RQ2	DQB1	DQB5	SIO1
4	GND	VDD	GND	GNDa	VDD	GND	VDD	VDD	GND
3	DQA7	DQA4	CFM	CFMN	RQ5	RQ3	DQB0	DQB4	DQB7
2									
1	GND		VDD				VDD		GND
	A	B	C	D	E	F	G	H	J

Figure 10b is "mirrored pinout" DRAM BGA.



Substrates contained in Multichip modules and system in package (SiP) benefit from optimization. The "substrate" of the SiP may be thought of as a miniature PC board. SiP designs can be optimized with interactive collaboration between chip designers and board designers. However, the foregoing optimization of SiP and Multichip modules is still performed within the definition of the Chip Packaging 1.0 environment; whereas, Chip Packaging 2.0 involves re-mapping IC package pinouts of legacy die, rather than new silicon designs.

CHIP PACKAGING 2.0 ISSUES

There are numerous issues yet to be solved before Chip Packaging 2.0 can be adopted as a standard industry practice.

Firstly, EDA chip pinout optimization software must be reliable and economically available for mainstream board designers to use. Sigrity demonstrated a version of such EDA chip optimization software during the June 2007 Design Automation Conference (DAC) in San Diego [5]. Another company, CAD Design Software demonstrated a version EDA chip optimization software during the July 2007 Semicon West show in San Francisco [6]. Other companies are working on creating versions of EDA chip optimization software.

Assuming that the foregoing issue with EDA software is resolved, the next challenge of Chip Packaging 2.0 is how to assemble die with crossing "bird's nest" wire bonding that go across the die in every direction. A hallmark of Chip Packaging 1.0 is the neat and orderly wire bonding. However, in the Chip Packaging 2.0 environment, "neat and orderly" is replaced with apparently disorderly wires that cross over one other as shown in Figure 11.

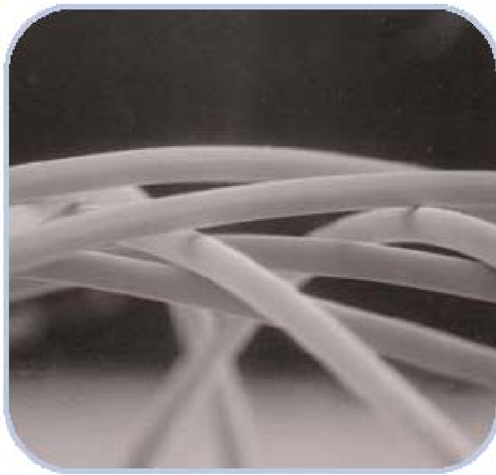


Figure 11. Example of insulated bonding wire that safely allows wires to cross.

A likely solution is to use Microbonds X-Wire insulated bonding wires [7]. Most late version bonding machines are easily converted to use insulated bonding wires. Figure 12 shows insulated bonding wires in an open cavity QFN package on display at July 2007 Semicon West by Tanaka Kikinzoku [8]. The QFN package was bonded using X-Wire insulated wires by Promex [9].

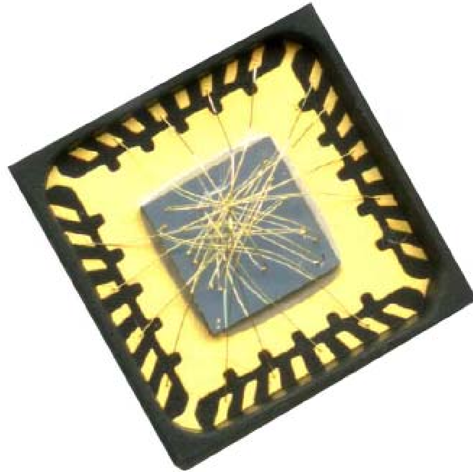


Figure 12. Example of a crossing insulated bonding wires in an open cavity QFN package.

Industry standard JEDEC IC package outlines such as QFN, QFP, SOIC, BGA, CSP, TSOP and the like are used in Chip Packaging 2.0.

The cumulative sum total thickness of crossing bonding wires cannot exceed the maximum "headroom" of the IC package. While there is no theoretical maximum number of wires that are allowed to cross, there is a practical limit to contend with. About 10 mils "headroom" is normally required between the upper most wire and the internal ceiling of the plastic IC package. Assuming that typical insulated bonding wire is 1mil in diameter, the maximum number of crossing wires is easily calculable, after taking into consideration the thickness of the die and thickness of the lead frame.

Economic issues need to be addressed. It is anticipated that early stage, low volume costs per device will be higher for Chip Packaging 2.0 assembly due to non-recurring development and device testing costs. However, it is anticipated that such initial higher costs will be offset by the lowering of raw material costs in PC Board (smaller boards, fewer inner layers, smaller cabinetry) and quicker time to market. Since resultant board designs will become simpler, it is anticipated that there will be a lowering of costs related to testing, rework and field failures.

Other issues involving grounding, shielding, cross talk and EMI need to be meted out and resolved.

Let's walk through a very simple circuit design. For purposes of discussion, figure 13 illustrates the "before" non-optimized board design. U1 and U2 are *off the shelf* 8 pin SOIC packages. The copper routing on the PC board from U1 pin 4 to U2 pin 7 crosses the copper routing from U1 pin 5 to U2 pin 8. To prevent short circuits, board designers would typically add a layer with plated vias to complete the design.

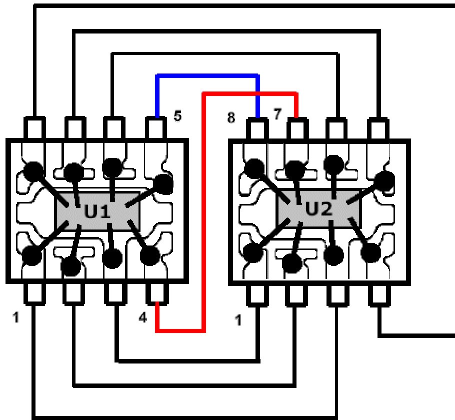


Figure 13. "Before" non-optimal board design.

Figure 14 illustrates an "after" optimized board with shorter copper routing, less plated vias and fewer layers. The "optimized" board is achieved by re-mapping the pinouts of U2**'** without changing the performance of the silicon die.

The board designer uses EDA chip pinout optimization software to simultaneously iterate and re-map U2**'** while auto routing copper traces on the board. After completing the iteration process, the EDA software determines that 2 bonding wires inside U2**'** should be remapped. The re-mapped U2**'** requires crossing of bonding wires from die pad 7 to lead frame pin 8 and from die pad 8 to lead frame pin 7.

The EDA software creates a bonding schedule (net list), and the data is presented to the IC packaging subcon to assemble the legacy die (or wafer). The wire-bonding machine employs the use of insulated bonding wires to prevent short circuits with the chip package.

U2**'** is delivered to the board assembler who uses standard SMT assembly practices to mount the components and complete the board assembly.

Though the above examples in Figure 13 and Figure 14 are simplistic, the same process is applied to complex board designs.

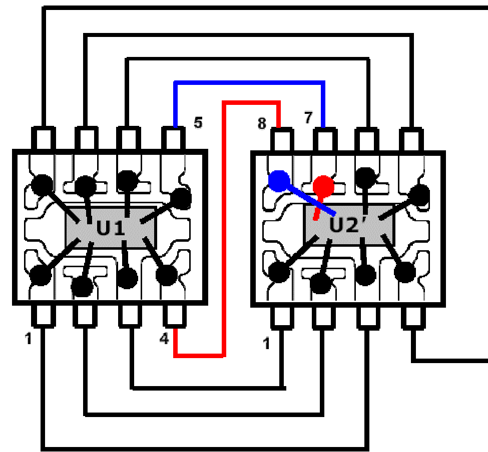


Figure 14. "After" optimal board design. U2**'** is re-mapped using insulated bonding wires to prevent shorting pins 7 and 8 with the IC package.

SUMMARY

This paper describes a means for empowering board designers to optimize board-level designs by re-mapping pinouts of legacy die in a proposed Chip Packaging 2.0 world.

It is observed that in the current Chip Packaging 1.0 environment, there is no communication channel for chip designers to collaborate with board designers. Further, it is observed that packaged chips are routinely thrown "over the wall" for board designers to deal with.

Thus, Mirror Semiconductor [10] poses the question *"what if"* board designers were empowered to re-map legacy package pinouts (without changing the performance of the silicon) in order to design optimum PC boards?

Suitable EDA software is the tipping point for ushering the onset of the Chip Packaging 2.0 world. Such software re-maps legacy chip pinouts while simultaneously optimizing the board, creates the requisite chip pinout-bonding schedule and seamlessly delivers it to wire bonding machines via the Internet (or by conventional means).

A willing and cooperative supply chain completes the cycle by delivering, on demand, "User Definable Pinout" (UDPo) according to the customer's (board designer's) requirements.

The author hopes that this paper stimulates thinking relative to the topic of Chip Packaging 2.0 and invites interested parties to continue further discussion.

ACKNOWLEDGEMENTS

The author extends copious amounts of credit to Joseph Fjelstad [11] for his imaginative "out of the box" suggestion that system designers should be empowered to define chip-packaging pinouts. I thank Charles Clark, Dr. Barry Moore, and Jerry Falwell, Jr. of Liberty University for sharing their enthusiasm for mirrored pinout packaging. I also thank TopLine Corporation [12] for their support and assistance to launch Mirror Semiconductor.

REFERENCE

[1] http://en.wikipedia.org/wiki/Speed_of_light

[2] US Patent 4,651,416. Inventor: Albert D. Paul, Filed Aug 26, 1985. Issue Date: Mar. 24, 1987

[3] All mainstream makers have "mirrored pinout" or "reversed pinout" DRAM, SRAM, etc.

[4] Micron Datasheet MT6V8M16R1-3M, et al Mirrored Pinout 62-pin FGBA. July 2000

[5] Sigrity (Santa Clara, California, USA)
Orbital IO Planner
www.sigrity.com

[6] CAD Design Software (San Jose, California, USA)
www.CAD-Design.com

[7] Microbonds (Markham, Ontario, Canada)
X-Wire insulated bonding wire White Paper. May 2006
www.microbonds.com

[8] Tanaka Kikinzoku (Japan)
www.tanaka.co.jp

[9] Promex (Santa Clara, California, USA)
www.promex-ind.com

[10] Mirror Semiconductor (Irvine, California, USA)
Martin Hart www.MirrorSemi.com

[11] Verdant Electronics (Sunnyvale, California, USA)
Joseph Fjelstad http://www.VerdantElectronics.com

[12] TopLine Corporation (Garden Grove, California)
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