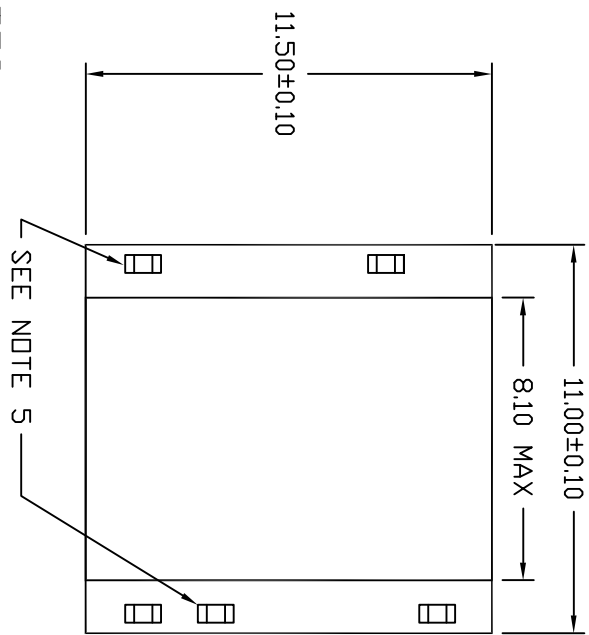
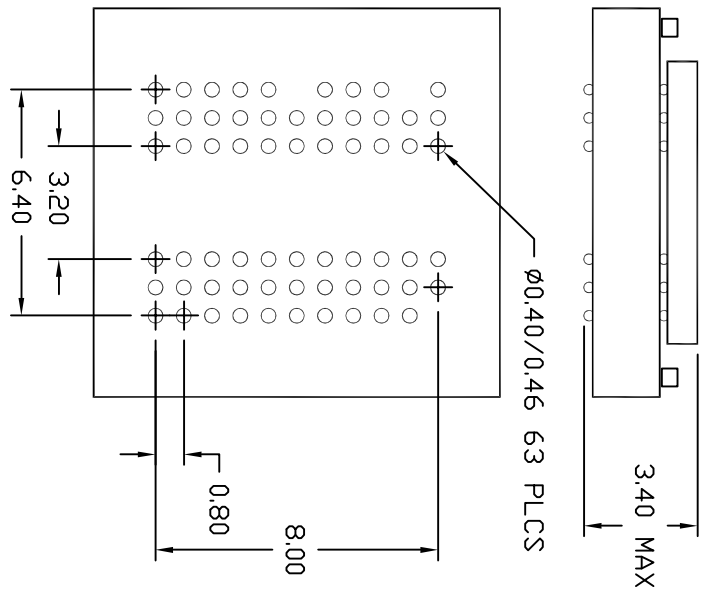


A	NEW	1/11/08	POW
REV	DESCRIPTION	DATE	APPROVAL

COMPONENT SIDE



BALL SIDE



- NOTES:
1. MAX FBGA COMPONENT SIZE: 8.1MM X 11.6 MM
 2. BALL ALLOY: 63/37 Sn/Pb
96.5/3.0/0.5 Sn/Ag/Cu
 3. BALL COPLANARITY: 0.10MM
 4. POWER AND GROUND PLANE CAN BE SPLIT INTO VDDQ AND VSSQ
 5. 5 CAPACITOR (0402) LOCATIONS ARE POSSIBLE. 2 LOCATIONS CAN BE FOR VDDQ/VSSQ
 6. ALL INTERNAL TRACES LENGTH ARE WITHIN 1%.
 7. INTERNAL CIRCUITRY IS DESIGN FOR 50 OHM IMPEDANCE.

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TOLERANCES UNLESS NOTED:		APPROVALS		DATE		
X.XXX	±	DRAWN	POW	10/16/07		
X.XXX	±	ENG				
X.XXX	±	REV				
ANGLES	±	QA				
ALL DIMENSIONS ARE IN DIMETERS		THIRD ANGLE PROJECTION:	SCALE	SIZE	DRAWING NO.	REV
			NONE	A	DDR2 StackChip	A
			DO NOT SCALE DRAWING	SHEET	1	OF 2

TITLE BGA COMPONENT STACK
DDR2 256Mb X 4 X 2 = 2Gb



A	NEW	1/11/08	POW
REV	DESCRIPTION	DATE	APPROVAL

A13	NC	L	NC	A12	VDD
VSS	A8	A11	A9	A7	
DDT1	A4	A6	A5	A3	VSS
VDD	A0	A2	A1	A10	CKE1
CS1	CS	CAS	BA1	BA0	NC
DDT	CHK	RAS	WE	CKE	
VDD	CHK	VSSL	VSS	VREF	VDDL
NC	VSSQ	DQ2	DQ3	VSSQ	NC
VDDQ	DQ0	VDDQ	VDDQ	DQ1	VDDQ
NC	VSSQ	DQS	DM	VSSQ	NC
VDDQ	DQS	VSSQ	VSS	NC	VDD

6 5 4 3 2 1

BALL SIDE

VIEW FROM TOP (SEE BALLS THROUGH PACKAGE)

TOLERANCES UNLESS NOTED:		APPROVALS		DATE	 Mirror Semiconductor™
X.XXX	±	DRAWN	POW	10/16/07	
X.XXX	±	ENG			
ANGLES	±	REVISED			
ALL DIMENSIONS ARE IN DIMETERS		THIRD ANGLE PROJECTION:	SCALE	SIZE	DRAWING NO.
			NONE	A	DDR2 StackChip
		REVISED	DO NOT SCALE DRAWING	SHEET	2 OF 2

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