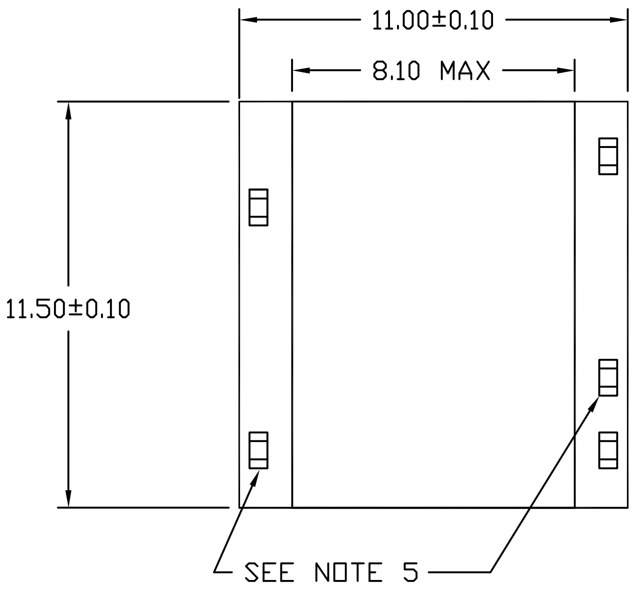
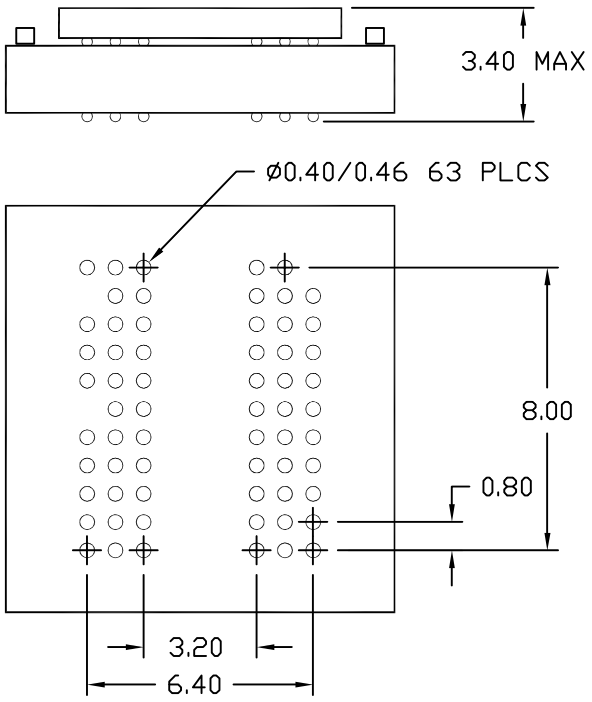
REV	DESCRIPTION	DATE	APPROVAL
A	NEW	1/11/08	POW

COMPONENT SIDE



BALL SIDE



NOTES:

1. MAX FBGA COMPONENT SIZE: 8.1MM X 11.6 MM
2. BALL ALLOY: 63/37 Sn/Pb
   96.5/3.0/0.5 Sn/Ag/Cu
3. BALL COPLANARITY: 0.10MM
4. POWER AND GROND PLANE CAN BE SPLIT INTO VDDQ AND VSSQ
5. 5 CAPACITOR (0402) LOCATIONS ARE POSSIBLE. 2 LOCATIONS CAN BE FOR VDDQ/VSSQ
6. ALL INTERNAL TRACES LENGTH ARE WITHIN 1%.
7. INTERNAL CIRCUITRY IS DESIGN FOR 50 OHM IMPEDANCE.

TOLERANCES UNLESS NOTED:	
X.XX	±
X.XXX	±
X.XXXX	±
ANGLES	±

ALL DIMENSIONS ARE IN: ☐ INCHES ☐ MILLIMETERS

THIRD ANGLE PROJECTION:

APPROVALS		DATE
DRAWN	POW	10/16/07
ENG		
MFG		
QA		
CUST		
REVISED		

Mirror Semiconductor ™

TITLE BGA COMPONENT STACK
DDR2 256Mb X 4 X 2 = 2Gb

SCALE	SIZE	DRAWING NO.	REV
NONE	A	DDR2 StackChip	A

DO NOT SCALE DRAWING

SHEET 1 OF 2

REV	DESCRIPTION	DATE	APPROVAL
A	NEW	1/11/08	POW

6	5	4		3	2	1
	A13	NC	L	NC	A12	VDD
VSS	A8	A11	K	A9	A7	
ODT1	A4	A6	J	A5	A3	VSS
VDD	A0	A2	H	A1	A10	CKE1
$\overline{\text{CS1}}$	$\overline{\text{CS}}$	$\overline{\text{CAS}}$	G	BA1	BA0	NC
ODT	$\overline{\text{CHK}}$	$\overline{\text{RAS}}$	F	$\overline{\text{WE}}$	CKE	
VDD	CHK	VSSL	E	VSS	VREF	VDDL
NC	VSSQ	DQ2	D	DQ3	VSSQ	NC
VDDQ	DQ0	VDDQ	C	VDDQ	DQ1	VDDQ
NC	VSSQ	DQS	B	DM	VSSQ	NC
VDDQ	$\overline{\text{DQS}}$	VSSQ	A	VSS	NC	VDD

6 5 4 3 2 1

BALL SIDE

VIEW FROM TOP (SEE BALLS THROUGH PACKAGE)

TOLERANCES UNLESS NOTED:	
X.XX	±
X.XXX	±
X.XXXX	±
ANGLES	±

ALL DIMENSIONS ARE IN:
☐ INCHES ☐ MILLIMETERS

THIRD ANGLE PROJECTION:

APPROVALS		DATE
DRAWN	POW	10/16/07
ENG		
MFG		
QA		
CUST		
REVISED		

Mirror
Semiconductor ™

TITLE BGA COMPONENT STACK
DDR2 256Mb X 4 X 2 = 2Gb

SCALE	SIZE	DRAWING NO.	REV
NONE	A	DDR2 StackChip	A

DO NOT SCALE DRAWING

SHEET 2 OF 2