

Improved PCB circuit design by Co-designing chips with User Definable Pinouts

By Martin Hart

INTRODUCTION

What if you could design ultimate boards simply by instructing your IC supplier to change the pinouts of the chips according to your needs? Today, that wish seems like a fairy-tale. Today's reality is that the semiconductor chip design team decides what type of IC package to use and how to assign the pinouts. Legacy IC package pinouts are cast in stone and defined in the chipmaker's datasheets. While some efforts exist to co-design new silicon designs and substrates (example: multichip modules, PoP and SiP), currently there is no method to change the pinouts of off-the-shelf die (wafers) according to the whim of the PC board designer. No communication channel exists between the chip design team and the PC board design team. IC packages are "tossed over-the-wall" to PC board designers who have the task to layout the board. The board designer has no ability to change any aspect of the IC package or to re-map the pinout. PC board designers are forced to accept the chips on the BOM. As a result, the board designer is unable to develop ultimate PC board designs. This current method is called "Chip Packaging 1.0" (Figure 1).

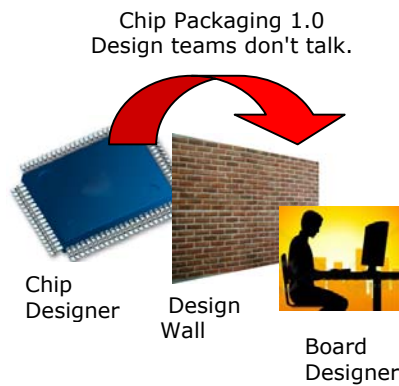


Figure 1. There is no collaboration between IC design team and system designers to change chip pinouts.

While there is a push to make co-design mainstream, there is little motivation for the IC design team to change. Improvement is possible if the semiconductor industry would adopt a new approach that offers more design freedom to the PC board designer, in the so called "Chip Packaging 2.0" environment. The new approach is compelling and worthy of consideration. In this new approach the PCB designer will use their EDA software to iterate the IC package pinouts of legacy IC die while simultaneously optimizing the board's routing (Figure 2.) This new approach to semiconductor packaging is referred to as "User Definable Pinout" (**UDPo**), which empowers board designers to re-map package pinouts of legacy chips using EDA software tools. The optimized chip is wire-bonded by the chipmaker according to the pinout instructions of the PC board designer. Once defined, the UDPo chip is added to the PC Board BOM (Bill of Materials) for mounting on PC boards using normal SMT assembly practices.

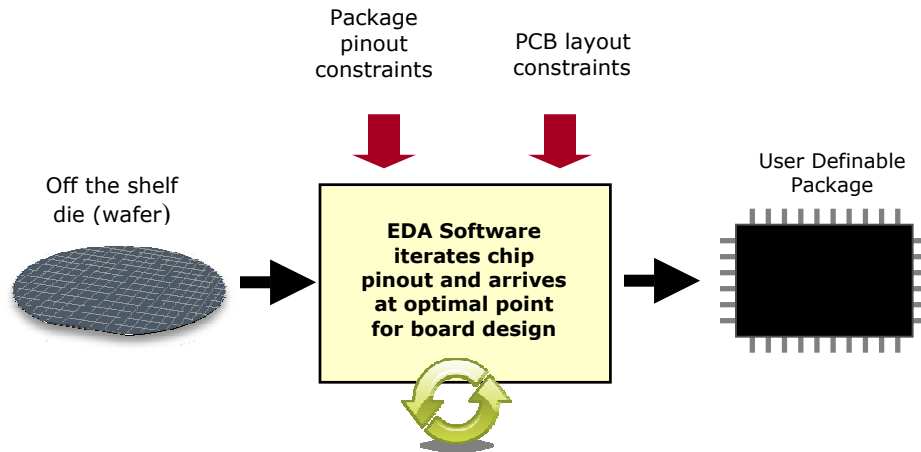


Figure 2. EDA software iterates UDPO - User Definable Package pinouts until PC board layout is optimized.

Typically during the circuit board’s initial design process, the board designer making a series of tradeoffs between electrical, thermal and mechanical needs. Once component locations are established, the circuit schematic is loaded and autorouting of the board commences. The iteration begins by benchmarking the initial results achieved with “standard pinout” packages. Next, the EDA software begins the pinout iteration process. Pairs of pinouts on selected IC packages are iterated while board routing is observed. During the iterative process, improvement is observed as copper routing lengths are shortened, board size is reduced and/or fewer inner layers are realized. Circuit speed improves roughly one nanosecond in a theoretical lossless substrate for each 6-inch (150mm) reduction of dual copper path (signal plus ground) according to the speed of light formula.

The remapping of the pinouts of one chip at a time is optimized. The co-design then cycles to the next chip until the total PC board is optimized to the satisfaction of the board designer. Once the chip pinouts are optimized, the EDA software will produce a bonding schedule (net list) for input into semiconductor wire-bonding machines. Chip packages are bonded using insulated bonding wire, to prevent shorting inside the IC package. The dream of creating single layer boards is within reach of possibility as shown in Figure 3.

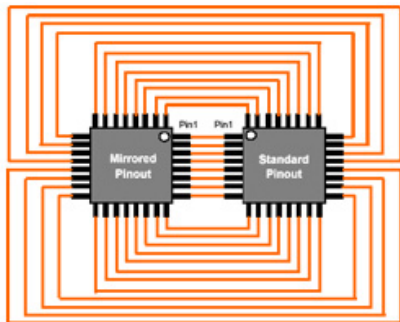


Figure 3. Single layer routing is possible when an optimize UDPO pinout device is bussed with standard IC.

Design Issues with UDPO

There are numerous issues yet to be solved before Chip Packaging 2.0 and user-definable pinouts can be adopted as a standard industry practice.

For example co-design EDA software tools for optimizing chip pinouts must be economical and reliable for mainstream board designers to use. Several companies are working on creating versions of EDA chip co-design and optimization software as demonstrated during the Design Automation Conference (DAC) and at the Semicon West show.

Assuming that reliability issues with EDA software can be resolved, the next challenge for the new approach to UDPO (user definable pinouts) is the collaboration with semiconductor makers. There is a need to define new libraries to allow silicon with unconventional wire bonding crossing over the die in every direction. Traditional wire bonding is very neat and orderly, however, in the proposed Chip Packaging 2.0 environment “neat and orderly” may need to be replaced with apparently disorderly wires that cross over one other (such as is enabled by Microbonds X-Wire insulated bonding wire) in order to achieve design optimization (see Figure 4).

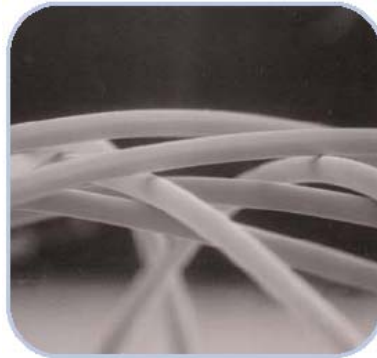


Figure 4. Example of insulated bonding wire that safely allows wires to cross.

Most of the common industry standard JEDEC IC package outlines such as QFN, QFP, SOIC, BGA, CSP, TSOP can all be adapted to the concept of UDPO. Standard wire bonding machines are easily converted to use insulated bonding wires. Figure 5 shows an extreme example of insulated bonding wires in an open cavity QFN package.

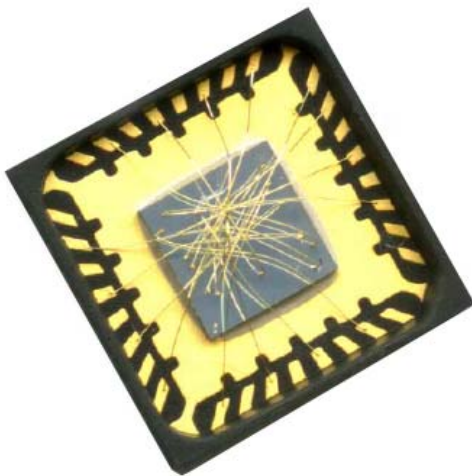


Figure 5. Example of an open cavity QFN package with crossing insulated bonding wires.

Designing with User Definable Pinouts

Let's examine a simple circuit design to illustrate how UDPo can improve design. Figure 6 shows the “before” non-optimized board design. U1 and U2 are *off the shelf* 8 pin SOP packages. The copper routing on the PC board from U1 pin 4 to U2 pin 7 crosses the copper routing from U1 pin 5 to U2 pin 8. The board designer will need to add a layer with plated vias to prevent short circuits and complete the design.

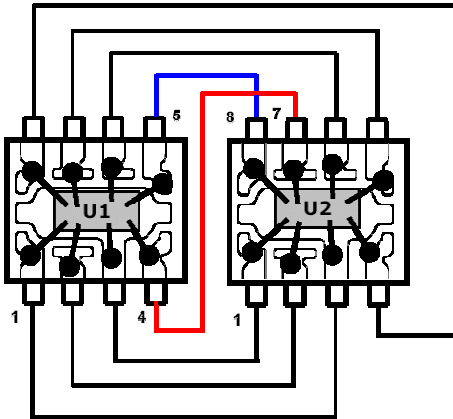


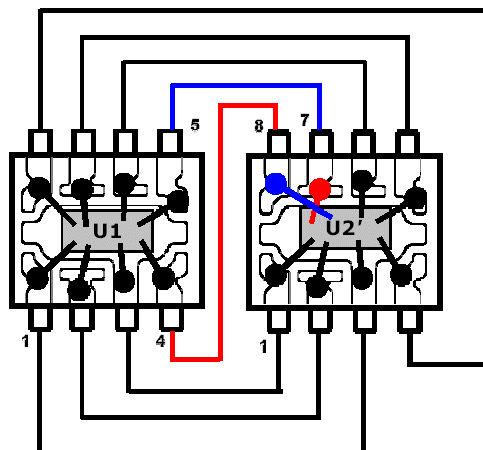
Figure 6. “Before” non-optimized board design.

By comparison, figure 7 illustrates the “after” “optimized” board achieved by re-mapping the pinouts of U2 without changing the performance of the silicon die. The optimized board requires no vias, has shorter copper routing and fewer layers.

The board designer will use co-design chip optimization EDA software to simultaneously iterate and re-map U2 while auto routing copper traces on the board. After completing the iteration process, the EDA software identifies that 2 bonding wires inside U2 should be remapped. The re-mapped U2 requires crossing of bonding wires from die pad 7 to lead frame pin 8 and from die pad 8 to lead frame pin 7.

The EDA software then creates a bonding schedule (net list), and the data is given to IC packaging assembler to wire bond the legacy die (or wafer). Insulated bonding wires are used to prevent short circuits with the chip package. The IC packaging assembler delivers U2 to the board assembler (EMS/CMS) who uses standard SMT assembly practices to mount the components and complete the board assembly. Admittedly, the above examples in Figure 7 and Figure 8 are ultra simplistic for illustration purposes only. However, the same co-design process can be applied to complex board designs. Since resultant board designs will become simpler, it is anticipated that there will be quicker time to market as well as lowering of costs related to testing, rework and field failures.

Figure 7. “After” optimized board design. U2 is re-mapped using insulated bonding wires to prevent shorting pins 7 and 8 with the IC package.



SUMMARY

Co-design is a compelling technique to empower printed circuit board designers to concurrently optimize board-level designs by re-mapping the pinouts of legacy die. Such EDA co-design software seamlessly delivers instructions to wire bonding machines via the Internet (or by conventional means) providing long-awaited benefits. In the current Chip Packaging 1.0 environment, there is no communication channel for board designers to collaborate with chip designers. However, there is an opportunity to change the way boards are designed in the future Chip Packaging 2.0 world. The “throw it over the wall” approach is not the best way to make designs. The question is “*what if*” board designers were empowered to re-map legacy package pinouts (without changing the performance of the silicon) in order to design optimum PC boards? Designers facing daily challenges shall have an active voice in providing enlightening answers to that question. Another question is what will it take to compel the semiconductor community to rally to the challenge of co-design with the new UDPo technology?

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