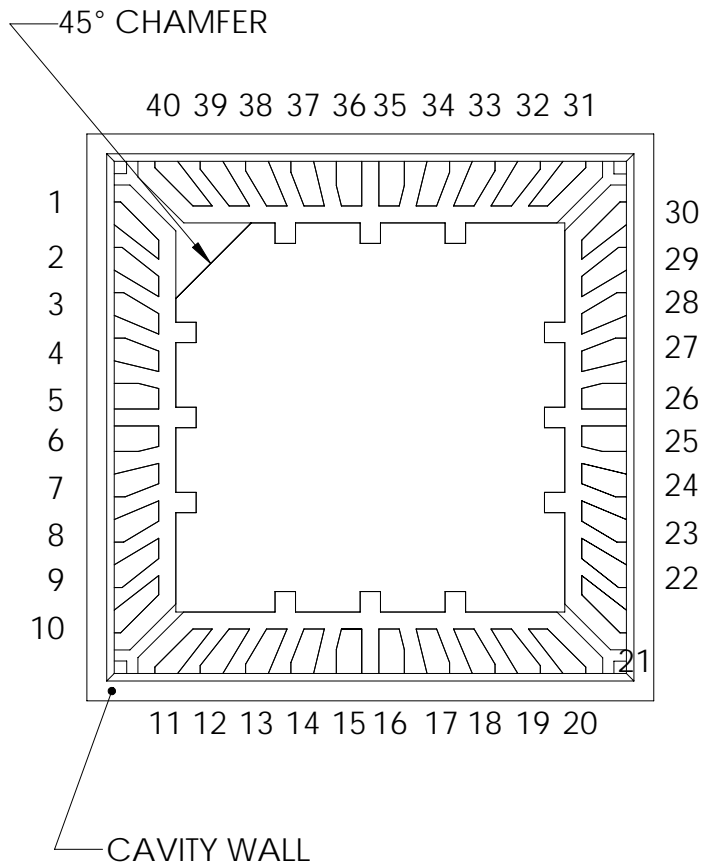
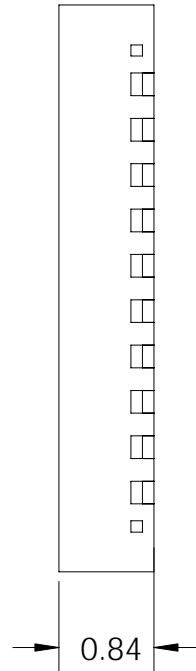




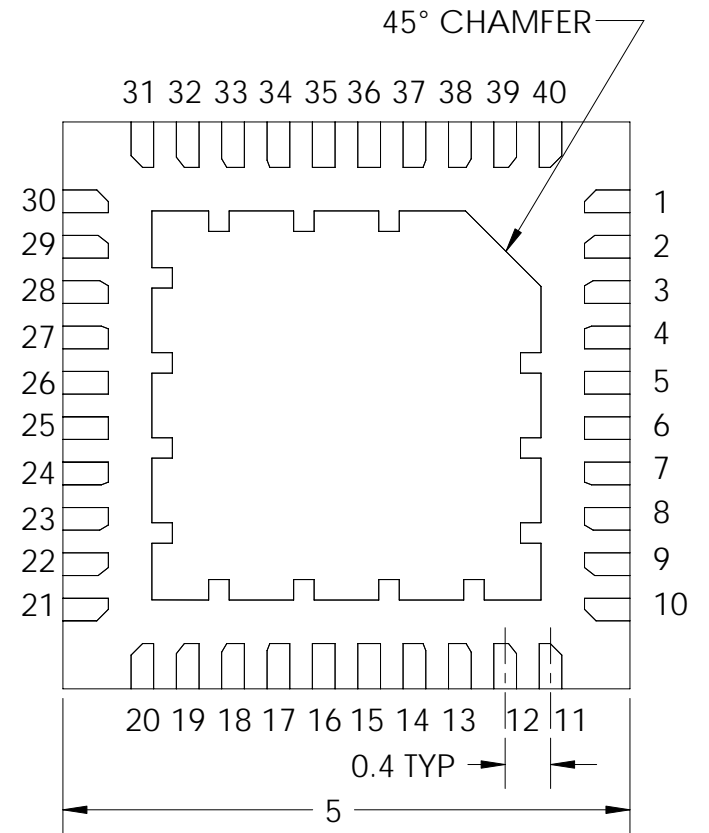
TOP VIEW



SIDE VIEW  
(BEFORE LID ATTACH)



BOTTOM VIEW



TITLE:

40-LEAD 5mm P=0.4 mm  
M-QFN CAVITY PACKAGE

SCALE  
**15:1**

SIZE  
**A**

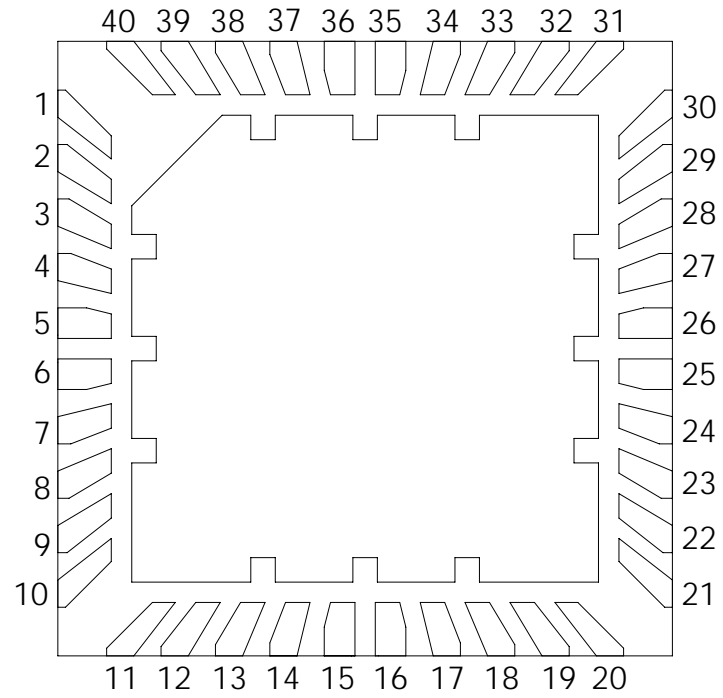
DWG. NO.  
**444050**  
**M-QFN40W.4**

REV  
**A**

DO NOT SCALE DRAWING

SHEET 2 OF 4

# BONDING DIAGRAM



**Mirror**  
Semiconductor™

TITLE:

40-LEAD 5mm P=0.4 mm  
M-QFN CAVITY PACKAGE

SCALE  
**18:1**

SIZE  
**A**

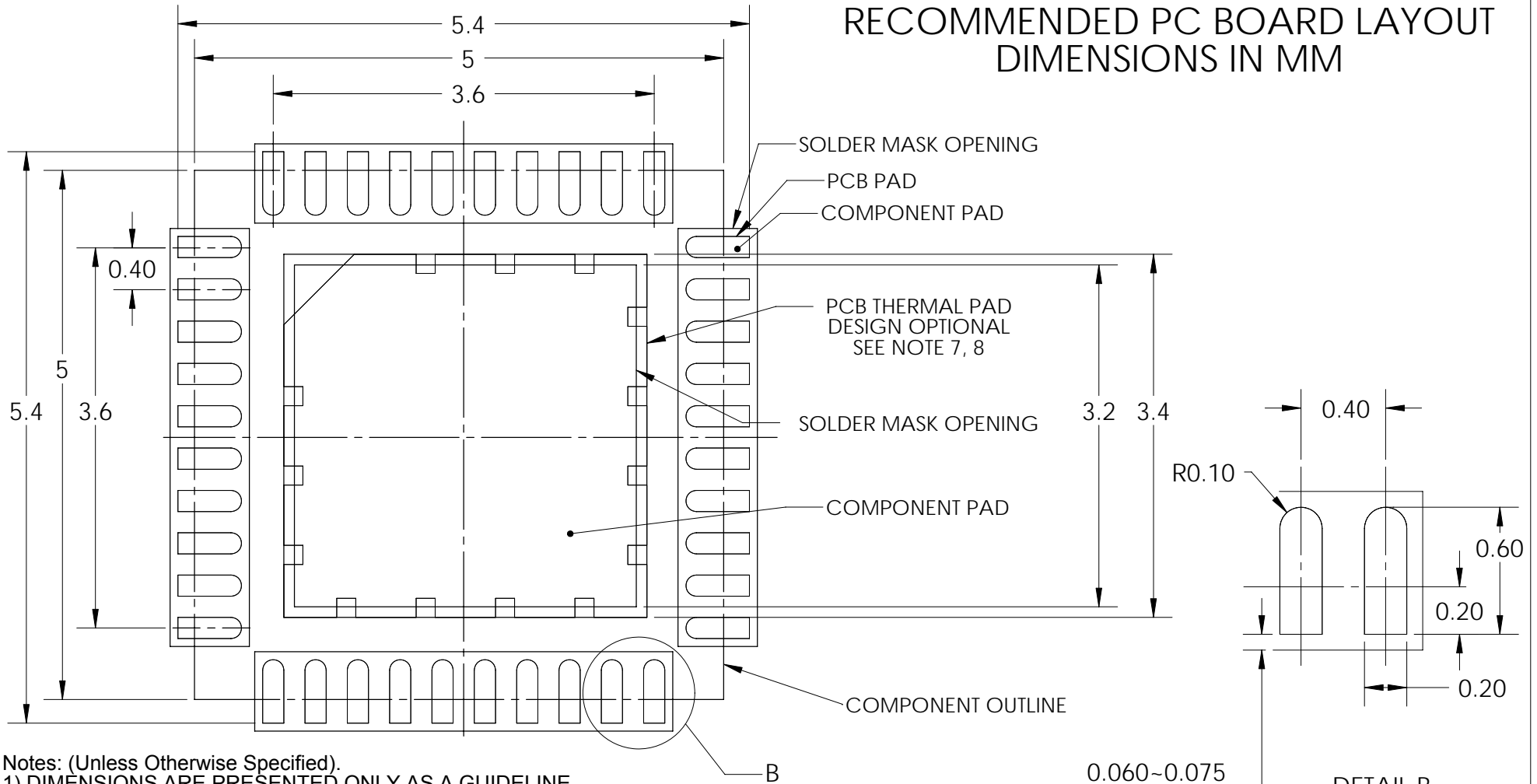
DWG. NO.  
**444050**  
**M-QFN40W.4**

REV  
**A**

DO NOT SCALE DRAWING

SHEET 3 OF 4

# RECOMMENDED PC BOARD LAYOUT DIMENSIONS IN MM



Notes: (Unless Otherwise Specified).

- 1) DIMENSIONS ARE PRESENTED ONLY AS A GUIDELINE. DESIGNERS SHOULD USE THEIR OWN KNOWLEDGE BASE WHEN DESIGNING THE PCB.
- 2) SURROUND EACH SIDE OF I/O PERIMETER PADS WITH 0.060~0.075 mm (NSMD) SOLDER MASK OPENING (2.4~3.0mils). OPTIONALLY OK TO USE RECTANGLE (NSMD) MASK OPENING AROUND I/O PADS.
- 3) ROUNDED PCB LAND PADS REDUCE SOLDER BRIDGING. PAD CHAMFER ANGLE MAY VARY
- 4) PCB LANDS SHOULD BE 0.2mm LONGER THAN THE PACKAGE I/O PADS.
- 5) THE WIDTH OF PERIMETER PCB PADS SHOULD MATCH (1:1) THE SAME WIDTH AS THE PACKAGE PADS.
- 6) REFER TO INDUSTRY REFERENCES SUCH AS IPC-SM-782 FOR PCB LAND PATTERN DESIGN.
- 7) THERMAL GROUND PADS MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
  - A. MAKE COPPER THERMAL PAD AS LARGE AS POSSIBLE.
  - B. DRILL MULTIPLE THERMAL VIAS 0.25~0.33mm DIAMETER USING 0.8~1.2mm PITCH GRID.
  - C. PLATE THERMAL VIA BARRELS WITH 1-OUNCE COPPER (18 $\mu$ m).
  - D. TENT (COVER) THERMAL VIAS WITH SOLDER MASK 0.1mm LARGER THEN THE VIA DIAMETER.
- 8) STENCIL DESIGN MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
  - A. LASER CUT STENCIL 0.125mm (5mil) THICK. APERTURE SIZE-TO-LAND RATIO OF 1:1.
  - B. THE SOLDER PASTE OPENING IN THE THERMAL PAD AREA SHOULD BE A MATRIX ARRAY OF SMALLER APERTURES INSTEAD OF ONE LARGE APERTURE TO CONTROL PASTE AMOUNTS.
  - C. APPLY 50% TO 80% SOLDER PASTE COVERAGE IN THE THERMAL PAD AREA.

0.060~0.075  
MASK OPENING

DETAIL B  
SCALE 36 : 1

**Mirror**  
Semiconductor™

TITLE:

40-LEAD 5mm P=0.4 mm  
M-QFN CAVITY PACKAGE

SCALE

**18:1**

SIZE

**A**

DWG. NO.

**444050  
M-QFN40W.4**

REV

**A**

DO NOT SCALE DRAWING

SHEET 4 OF 4