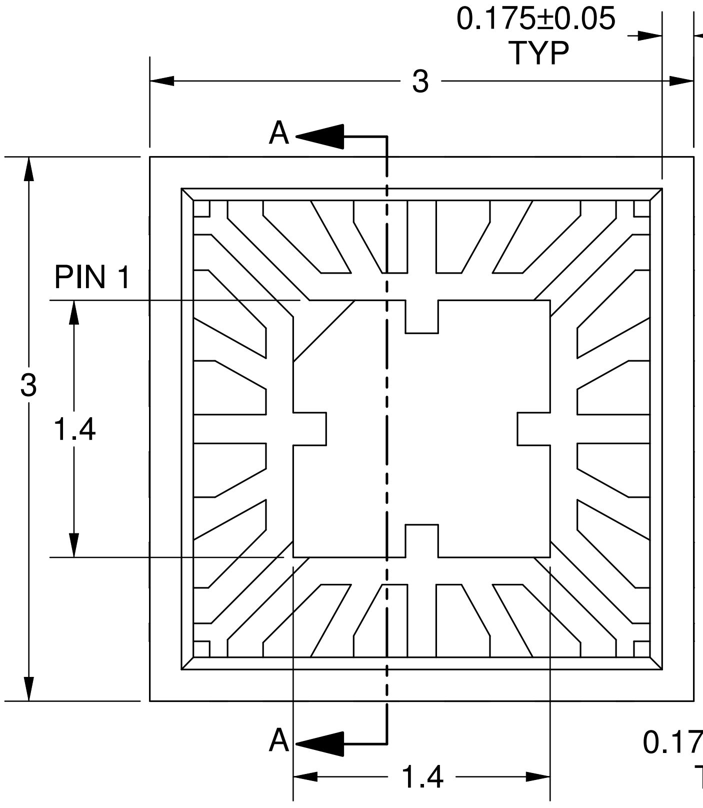
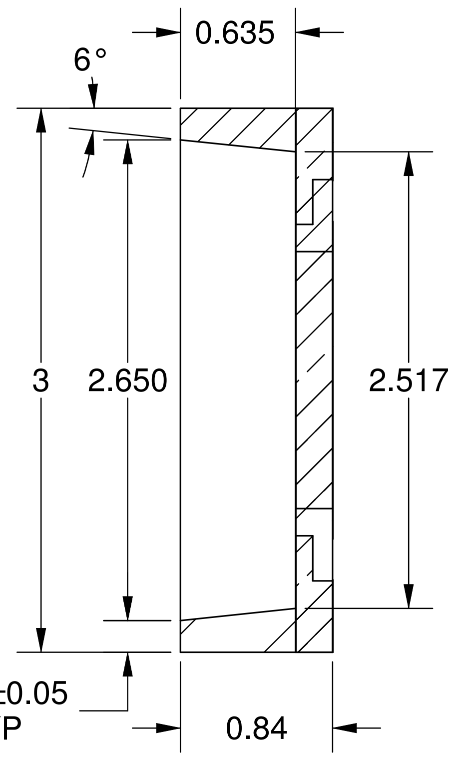
REVISIONS				
DATE	REV.	ECO	DESCRIPTION	APPROVED

TOP VIEW

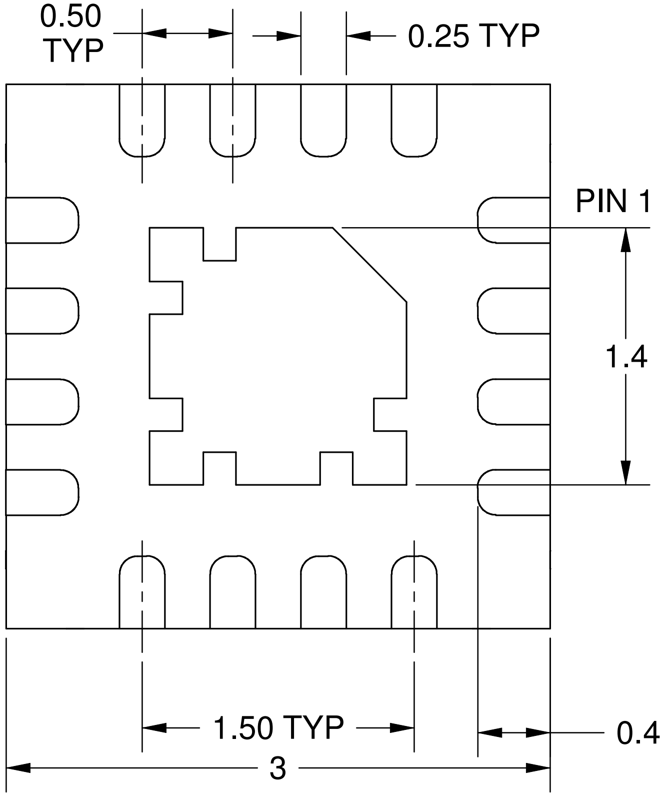


SIDE VIEW



SECTION A-A

BOTTOM VIEW



Notes: (Unless Otherwise Specified).
1) BODY: PLASTIC, SEMICONDUCTOR GRADE.
2) LEAD FRAME: COPPER, C-194 F/H.
3) LEAD FRAME PLATING: Ni, Pd, Au.
4) FRAME THICKNESS: 0.203MM.
5) DIE PAD: 1.4 X 1.4MM.
6) JEDEC OUTLINE: MO-220.
7) DIMENSIONS: MM.

PLATING THICKNESS

Ni	NICKEL	0.50-2.00 µm
Pd	PALLADIUM	0.02-0.15 µm
Au	GOLD	0.003-0.015 µm

OPTIONS AND ACCESSORIES:

DWG	PART #	SINGLE/ARRAY	DESCRIPTION
451650	M-QFN16W.5	SINGLE	SUBSTRATE WITH CAVITY WALL
451651	FA-QFN16P.5	ARRAY	SUBSTRATE WITHOUT CAVITY WALL
451652	F-QFN16W.5	SINGLE	SUBSTRATE WITHOUT CAVITY WALL
451656	MA-QFN16P.5	ARRAY	SUBSTRATE WITH CAVITY WALL
203050	M-CAP3	SINGLE	DOME LID FOR 451652
203051	FA-LID3	ARRAY	FLAT LID FOR 451656
203052	F-LID3	SINGLE	FLAT LID FOR 451650
203056	MA-CAP3	ARRAY	DOME LID FOR 451651

TOLERANCE UNLESS NOTED		
X.XX	+/-	0.01
X.XXX	+/-	0.005
X.XXXX	+/-	0.0005
ANGLES	+/-	0.5°

ALL DIMENSIONS IN
☒ INCHES ☐ MILLIMETERS

THIRD ANGLE PROJECTION

APPROVALS		DATE
DRAWN	J. Hines	6/14/2010
ENG		
MFG		
QA		
CUST		
REVISED		

Mirror
Semiconductor™

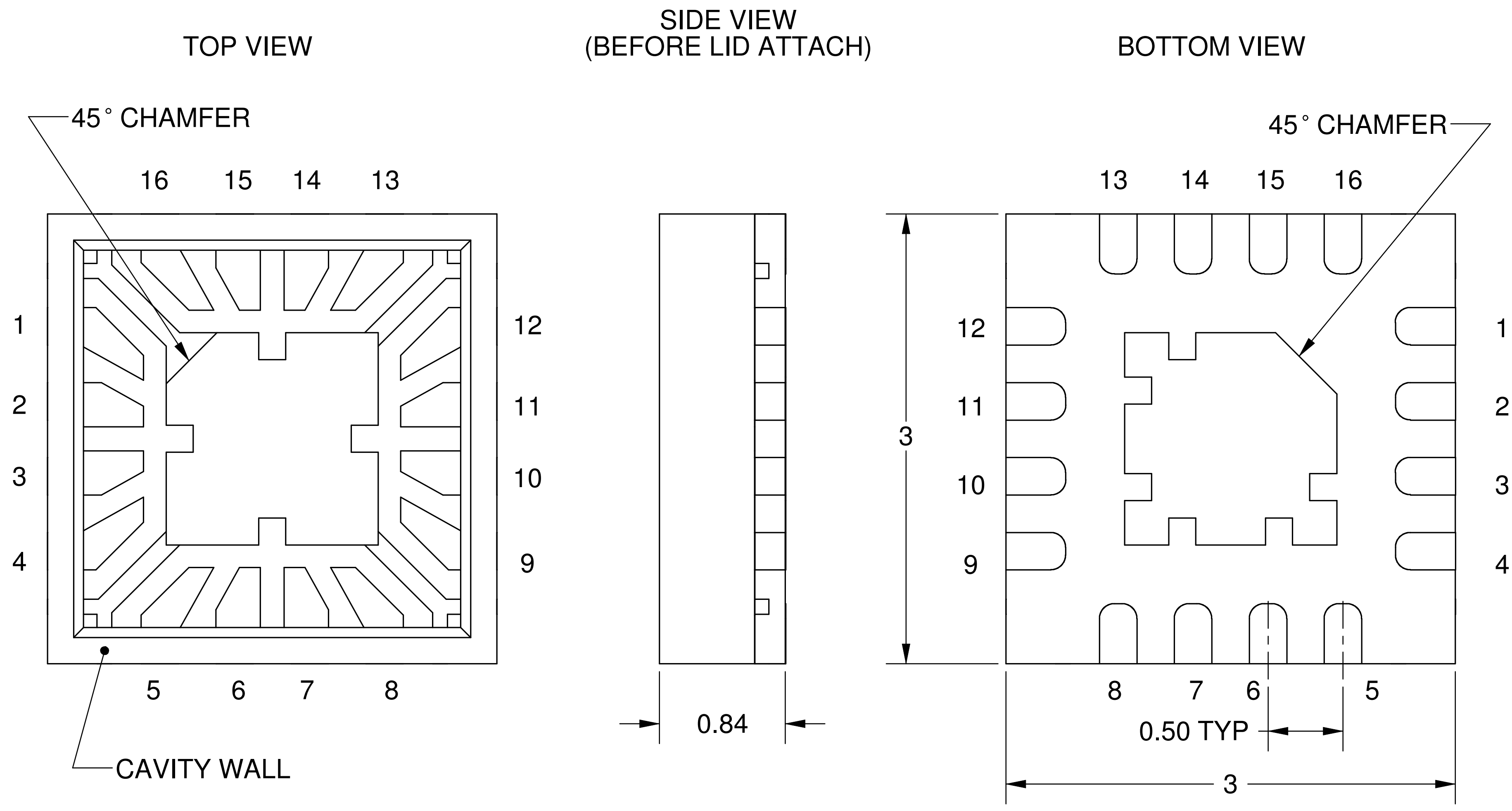
TITLE 16-LEAD 3mm P=0.5 mm
M-QFN CAVITY PACKAGE

SCALE	SIZE	DRAWING NO.	REV
24:1	A	451650	A

DO NOT SCALE DRAWING

SHEET 1 OF 4

PIN LOCATIONS


TOP VIEW

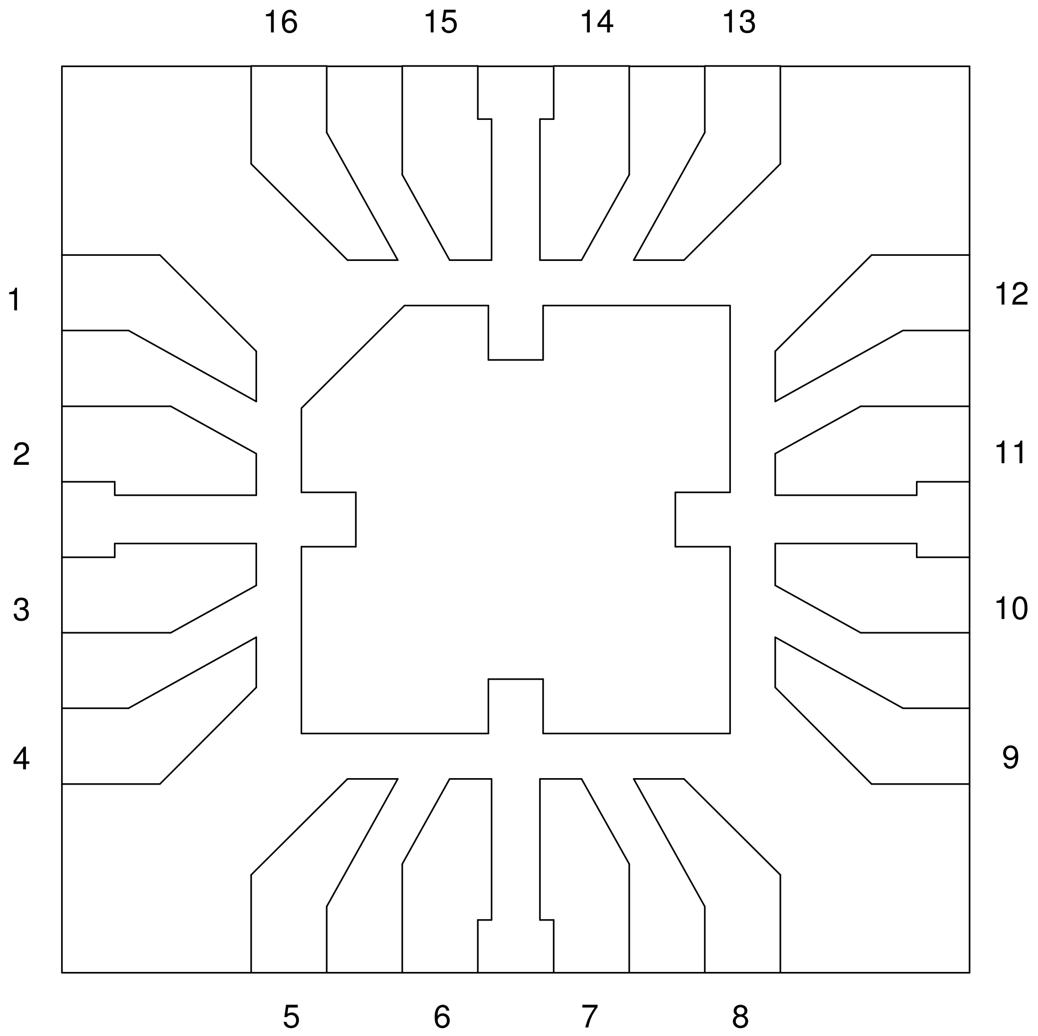
SIDE VIEW
(BEFORE LID ATTACH)

BOTTOM VIEW

Mirror
Semiconductor™

TITLE 16-LEAD 3mm P=0.5 mm M-QFN CAVITY PACKAGE			
SCALE 24:1	SIZE A	DRAWING NO. 451650	REV A
DO NOT SCALE DRAWING		SHEET 2 OF 4	

BONDING DIAGRAM



Mirror Semiconductor™

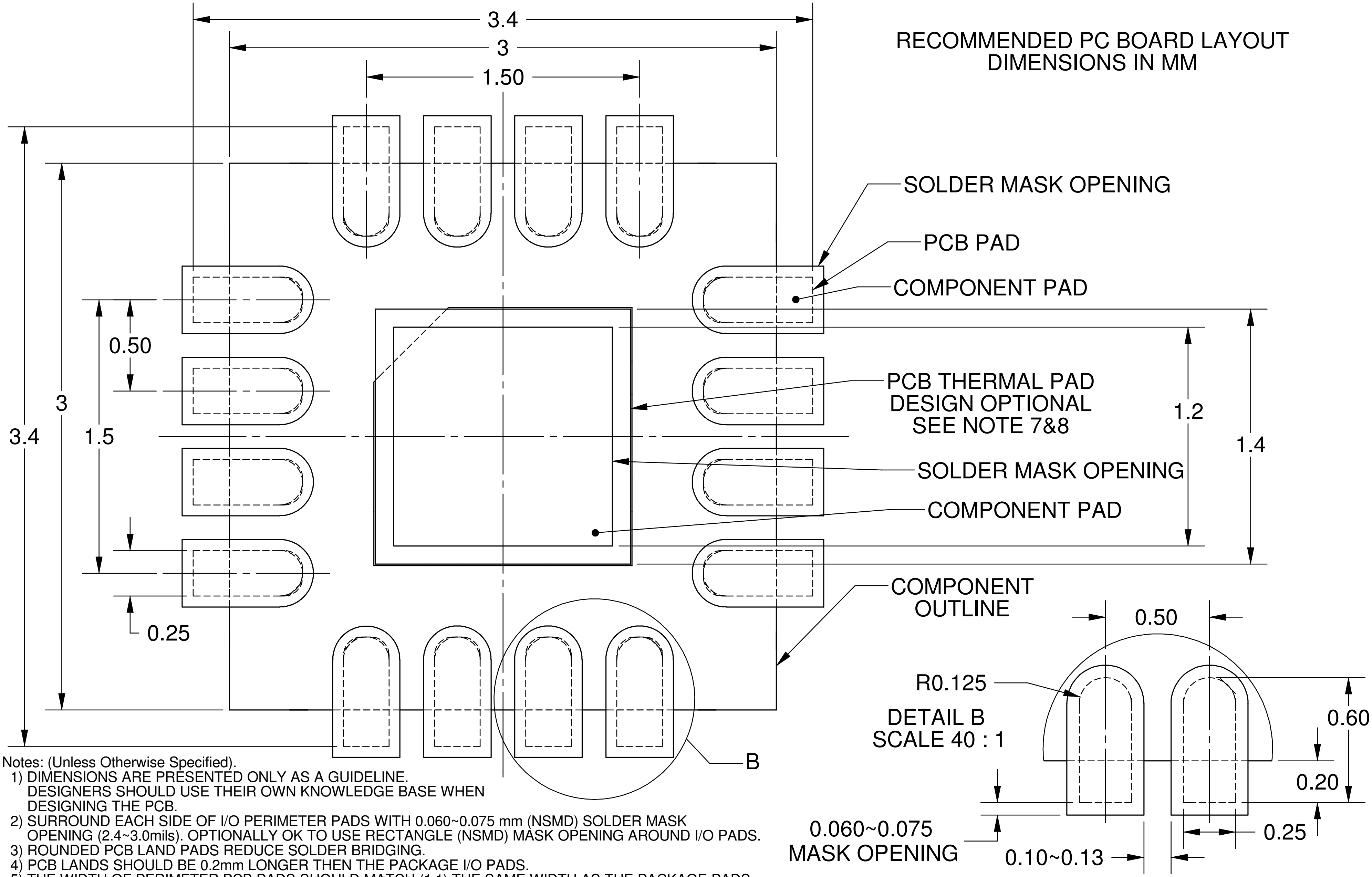
TITLE 16-LEAD 3mm P=0.5 mm
M-QFN CAVITY PACKAGE

SCALE	SIZE	DRAWING NO.	REV
40:1	A	451650	A

DO NOT SCALE DRAWING

SHEET 3 OF 4

RECOMMENDED PC BOARD LAYOUT
DIMENSIONS IN MM



Notes: (Unless Otherwise Specified).

1) DIMENSIONS ARE PRESENTED ONLY AS A GUIDELINE. DESIGNERS SHOULD USE THEIR OWN KNOWLEDGE BASE WHEN DESIGNING THE PCB.
2) SURROUND EACH SIDE OF I/O PERIMETER PADS WITH 0.060~0.075 mm (NSMD) SOLDER MASK OPENING (2.4~3.0mils). OPTIONALLY OK TO USE RECTANGLE (NSMD) MASK OPENING AROUND I/O PADS.
3) ROUNDED PCB LAND PADS REDUCE SOLDER BRIDGING.
4) PCB LANDS SHOULD BE 0.2mm LONGER THEN THE PACKAGE I/O PADS.
5) THE WIDTH OF PERIMETER PCB PADS SHOULD MATCH (1:1) THE SAME WIDTH AS THE PACKAGE PADS.
6) REFER TO INDUSTRY REFERENCES SUCH AS IPC-SM-782 FOR PCB LAND PATTERN DESIGN.
7) THERMAL GROUND PADS MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
    A. MAKE COPPER THERMAL PAD AS LARGE AS POSSIBLE.
    B. DRILL MULTIPLE THERMAL VIAS 0.25~0.33mm DIAMETER USING 0.8~1.2mm PITCH GRID.
    C. PLATE THERMAL VIA BARRELS WITH 1-OUNCE COPPER (18µm).
    D. TENT (COVER) THERMAL VIAS WITH SOLDER MASK 0.1mm LARGER THEN THE VIA DIAMETER.
8) STENCIL DESIGN MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
    A. LASER CUT STENCIL 0.125mm (5mil) THICK. APERTURE SIZE-TO-LAND RATIO OF 1:1.
    B. THE SOLDER PASTE OPENING IN THE THERMAL PAD AREA SHOULD BE A MATRIX ARRAY OF SMALLER APERTURES INSTEAD OF ONE LARGE APERTURE TO CONTROL PASTE AMOUNTS.
    C. APPLY 50% TO 80% SOLDER PASTE COVERAGE IN THE THERMAL PAD AREA.

Mirror Semiconductor™			
TITLE 16-LEAD 3mm P=0.5 mm M-QFN CAVITY PACKAGE			
SCALE 35:1	SIZE A	DRAWING NO. 451650	REV A
DO NOT SCALE DRAWING		SHEET 4 OF 4	