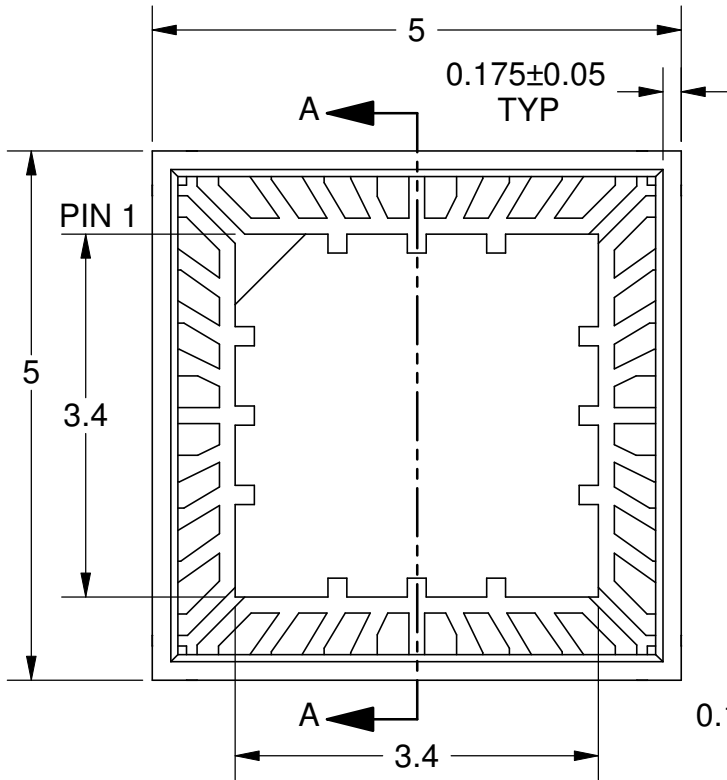
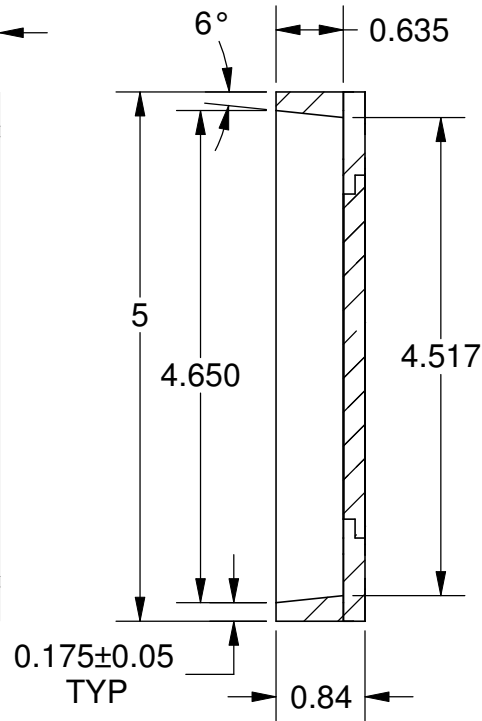


REVISIONS				
DATE	REV.	ECO	DESCRIPTION	APPROVED

TOP VIEW

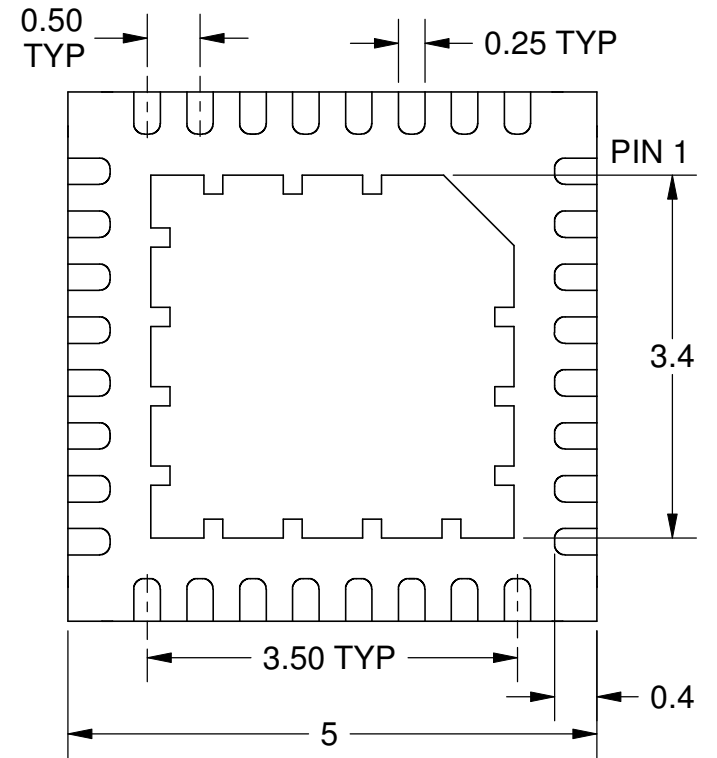


SIDE VIEW



SECTION A-A


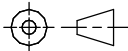
BOTTOM VIEW



- Notes: (Unless Otherwise Specified).
 1) BODY: PLASTIC, SEMICONDUCTOR GRADE.
 2) LEAD FRAME: COPPER, C-194 F/H.
 3) LEAD FRAME PLATING: Ni, Pd, Au.
 4) FRAME THICKNESS: 0.203MM.
 5) DIE PAD: 3.4 X 3.4MM.
 6) JEDEC OUTLINE: MO-220.
 7) DIMENSIONS: MM.

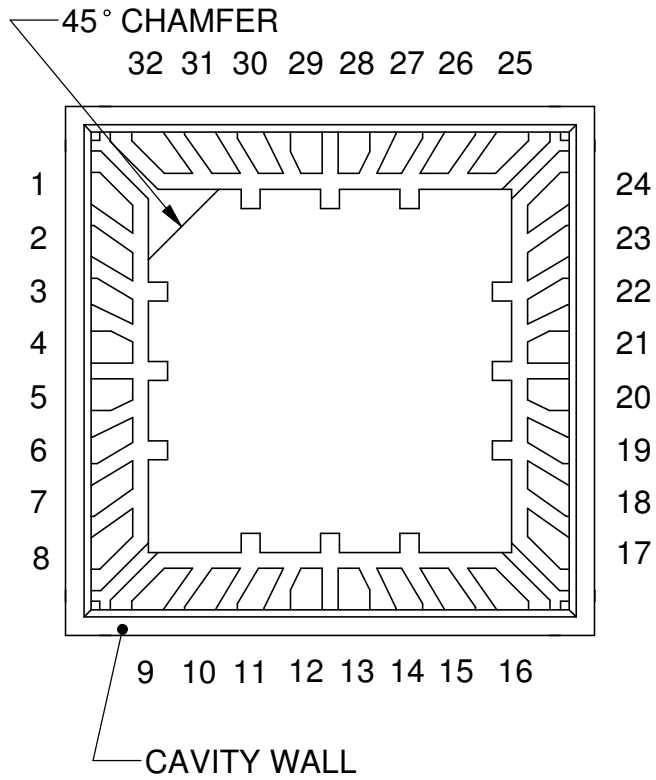
PLATING THICKNESS		
Ni	NICKEL	0.50-2.00 μm
Pd	PALLADIUM	0.02-0.15 μm
Au	GOLD	0.003-0.015 μm

OPTIONS AND ACCESSORIES:			
DWG	PART #	SINGLE/ARRAY	DESCRIPTION
453250	M-QFN32W.5	SINGLE	SUBSTRATE WITH CAVITY WALL
453251	FA-QFN32P.5	ARRAY	SUBSTRATE WITHOUT CAVITY WALL
453252	F-QFN32W.5	SINGLE	SUBSTRATE WITHOUT CAVITY WALL
453256	MA-QFN32P.5	ARRAY	SUBSTRATE WITH CAVITY WALL
205050	M-CAP5	SINGLE	DOMED LID FOR 453252
205051	FA-LID5	ARRAY	FLAT LID FOR 453256
205052	F-LID5	SINGLE	FLAT LID FOR 453250
205056	MA-CAP5	ARRAY	DOMED LID FOR 453251

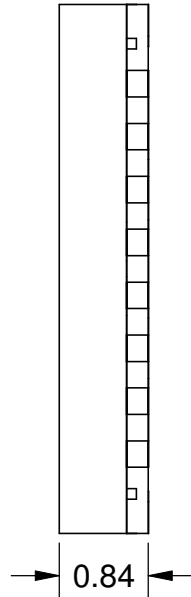
TOLERANCE UNLESS NOTED		APPROVALS	DATE	 Mirror Semiconductor™			
X.XX	+/- 0.01						
X.XXX	+/- 0.005						
X.XXXX	+/- 0.0005						
ANGLES	+/- 0.5°	ENG		SCALE	SIZE	DRAWING NO.	REV
ALL DIMENSIONS IN		MFG		14:1	A	453250	A
<input checked="" type="checkbox"/> INCHES	<input type="checkbox"/> MILLIMETERS	QA		DO NOT SCALE DRAWING			
THIRD ANGLE PROJECTION		CUST		SHEET 1 OF 4			
		REVISED					

PIN LOCATIONS

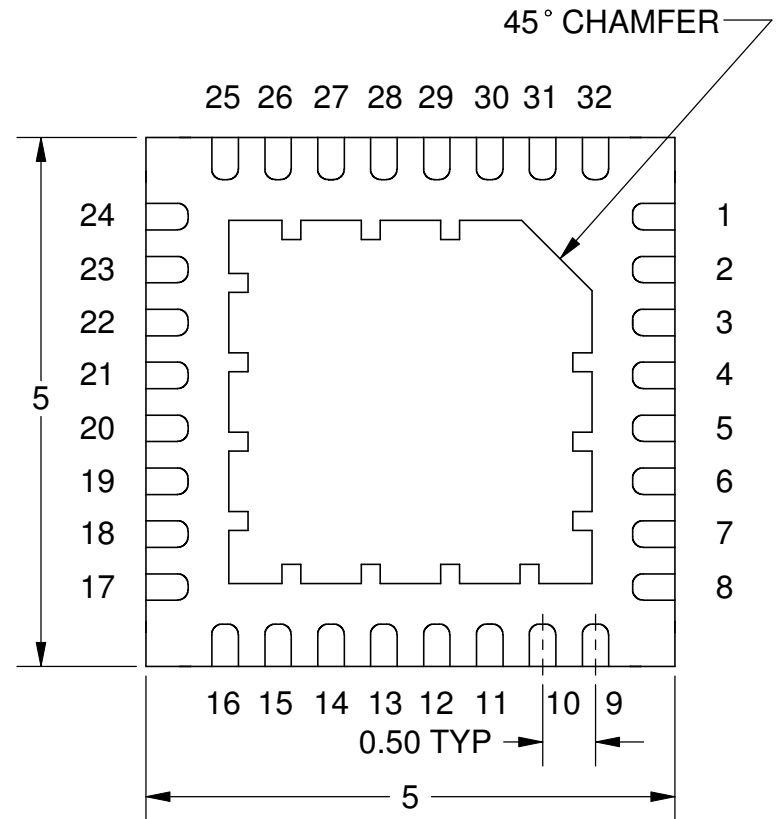
TOP VIEW



SIDE VIEW
(BEFORE LID ATTACH)



BOTTOM VIEW



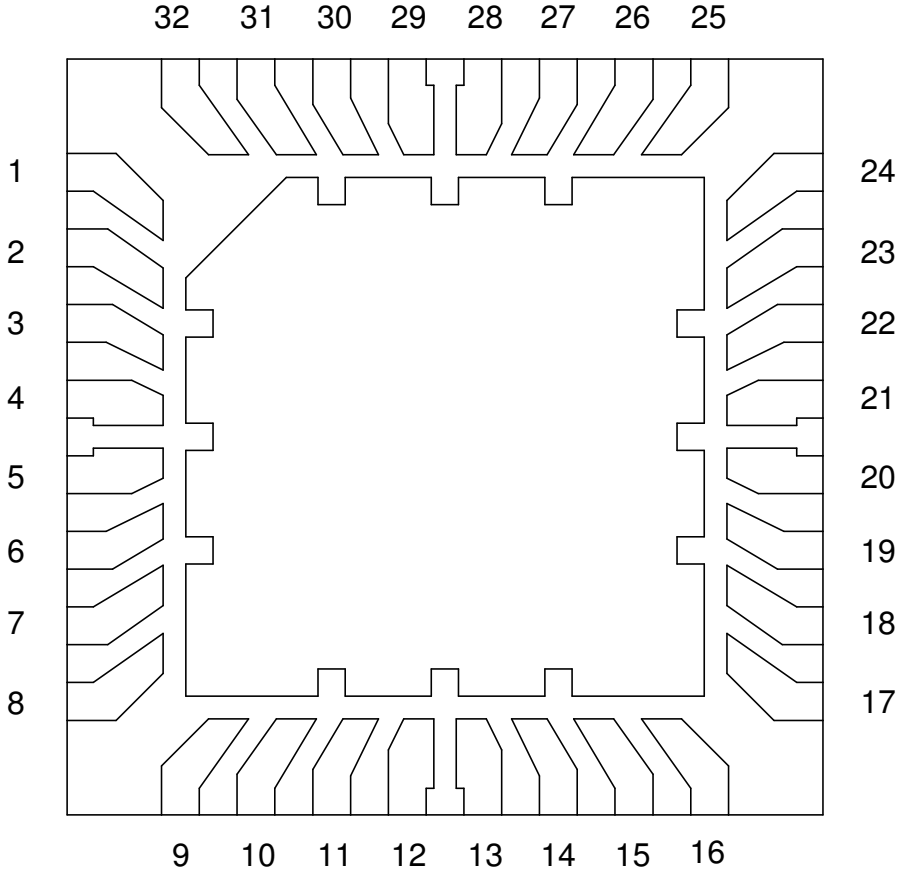
TITLE 32-LEAD 5mm P=0.5 mm
M-QFN CAVITY PACKAGE


SCALE 14:1	SIZE A	DRAWING NO. 453250	REV A
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DO NOT SCALE DRAWING

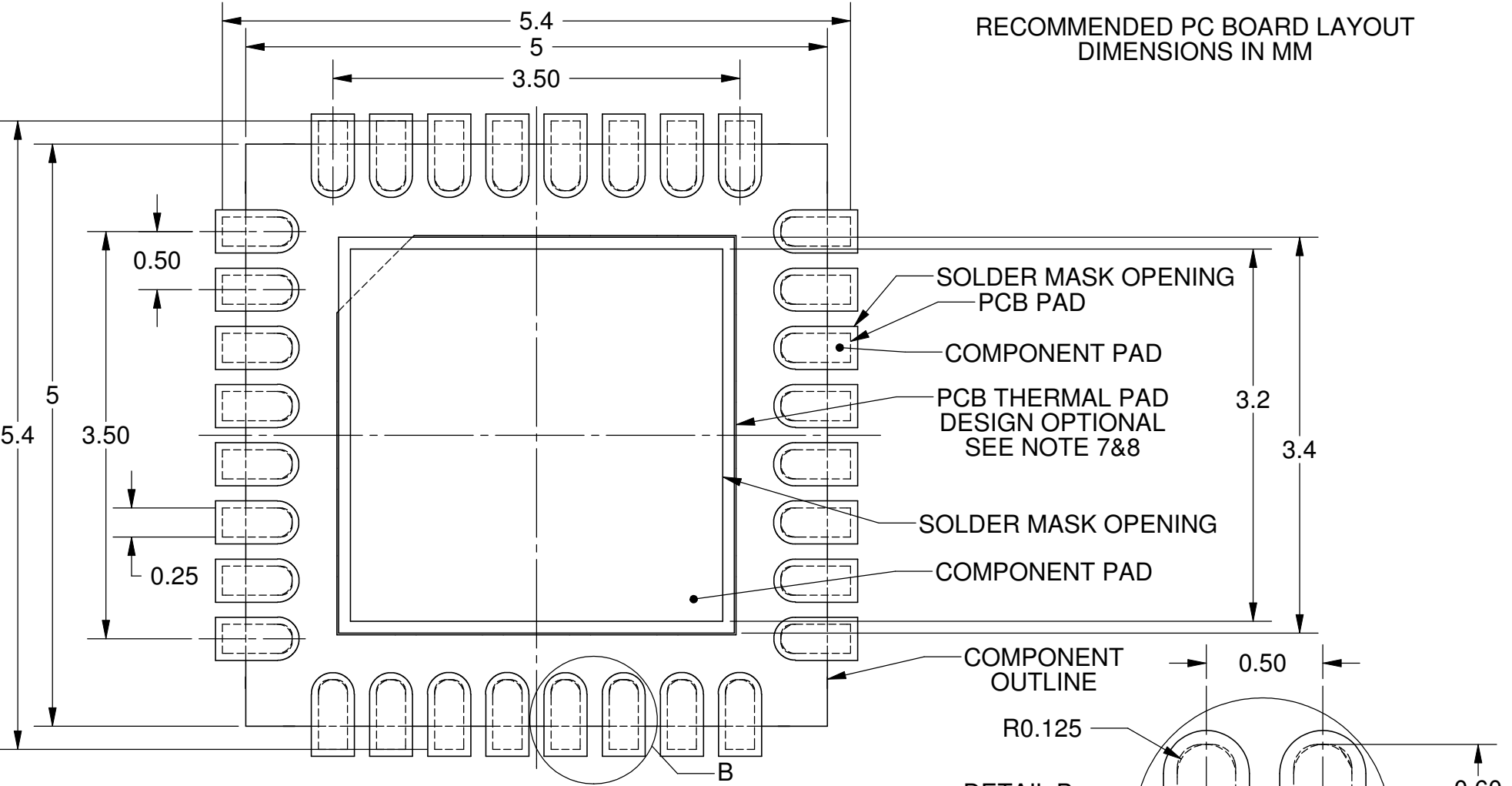
SHEET 2 OF 4

BONDING DIAGRAM

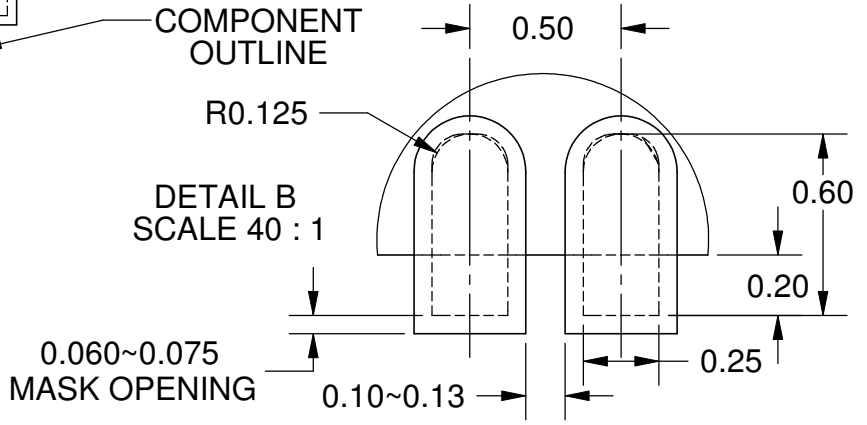


			
TITLE 32-LEAD 5mm P=0.5 mm M-QFN CAVITY PACKAGE			
SCALE 20:1	SIZE A	DRAWING NO. 453250	REV A
DO NOT SCALE DRAWING		SHEET 3 OF 4	

RECOMMENDED PC BOARD LAYOUT
DIMENSIONS IN MM



- Notes: (Unless Otherwise Specified).
- 1) DIMENSIONS ARE PRESENTED ONLY AS A GUIDELINE. DESIGNERS SHOULD USE THEIR OWN KNOWLEDGE BASE WHEN DESIGNING THE PCB.
 - 2) SURROUND EACH SIDE OF I/O PERIMETER PADS WITH 0.060~0.075 mm (NSMD) SOLDER MASK OPENING (2.4~3.0mils). OPTIONALLY OK TO USE RECTANGLE (NSMD) MASK OPENING AROUND I/O PADS.
 - 3) ROUNDED PCB LAND PADS REDUCE SOLDER BRIDGING.
 - 4) PCB LANDS SHOULD BE 0.2mm LONGER THEN THE PACKAGE I/O PADS.
 - 5) THE WIDTH OF PERIMETER PCB PADS SHOULD MATCH (1:1) THE SAME WIDTH AS THE PACKAGE PADS.
 - 6) REFER TO INDUSTRY REFERENCES SUCH AS IPC-SM-782 FOR PCB LAND PATTERN DESIGN.
 - 7) THERMAL GROUND PADS MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
 - A. MAKE COPPER THERMAL PAD AS LARGE AS POSSIBLE.
 - B. DRILL MULTIPLE THERMAL VIAS 0.25~0.33mm DIAMETER USING 0.8~1.2mm PITCH GRID.
 - C. PLATE THERMAL VIA BARRELS WITH 1-OUNCE COPPER (18µm).
 - D. TENT (COVER) THERMAL VIAS WITH SOLDER MASK 0.1mm LARGER THEN THE VIA DIAMETER.
 - 8) STENCIL DESIGN MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
 - A. LASER CUT STENCIL 0.125mm (5mil) THICK. APERTURE SIZE-TO-LAND RATIO OF 1:1.
 - B. THE SOLDER PASTE OPENING IN THE THERMAL PAD AREA SHOULD BE A MATRIX ARRAY OF SMALLER APERTURES INSTEAD OF ONE LARGE APERTURE TO CONTROL PASTE AMOUNTS.
 - C. APPLY 50% TO 80% SOLDER PASTE COVERAGE IN THE THERMAL PAD AREA.



Mirror Semiconductor™			
TITLE 32-LEAD 5mm P=0.5mm M-QFN CAVITY PACKAGE			
SCALE	SIZE	DRAWING NO.	REV
20:1	A	453250	A
DO NOT SCALE DRAWING			SHEET 4 OF 4