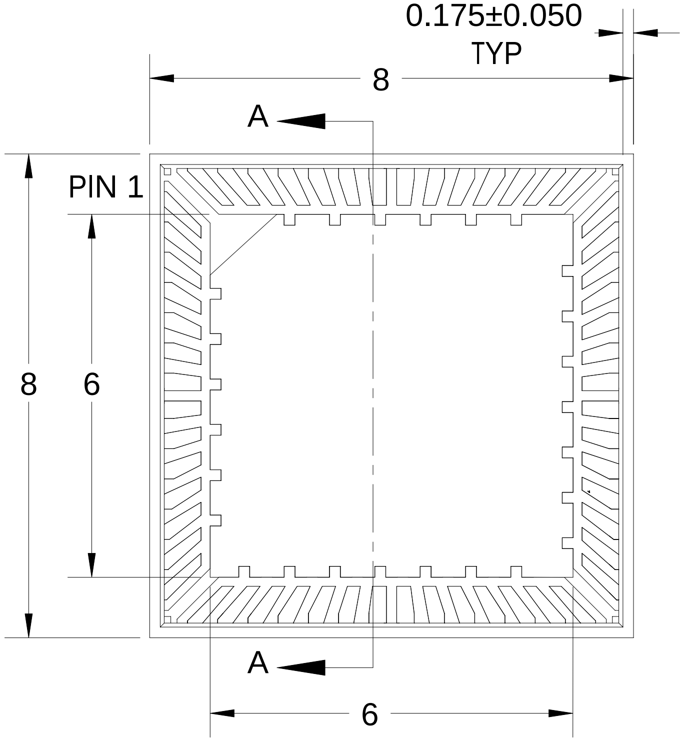
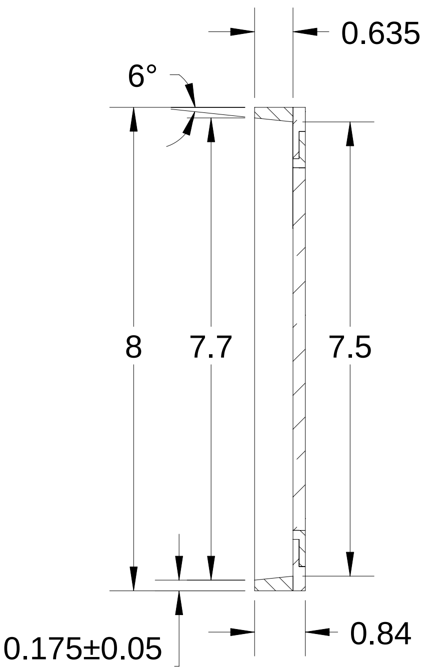
TOP VIEW

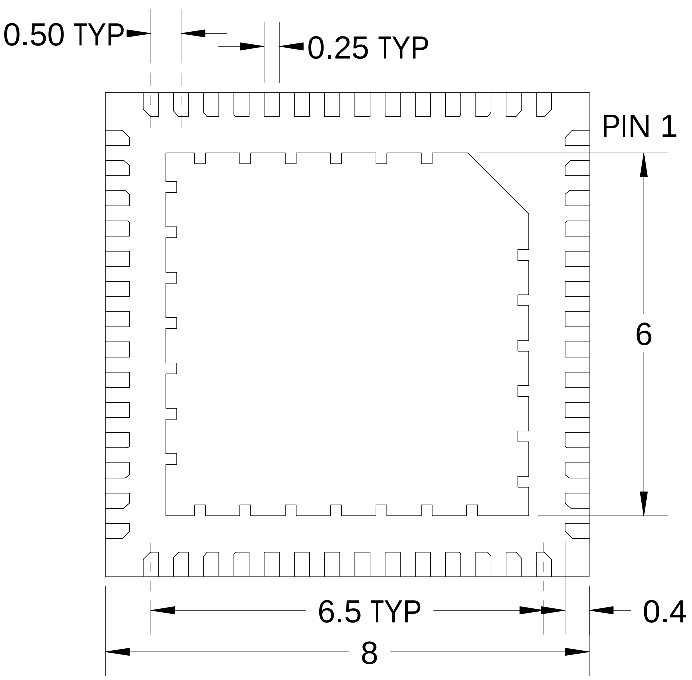


SIDE VIEW



SECTION A-A
SCALE 8 : 1

BOTTOM VIEW



Notes: (Unless Otherwise Specified)
1) BODY; PLASTIC, SEMICONDUCTOR GRADE
2) LEAD FRAME: COPPER, C-194F/H
3) LEAD FRAME PLATING: Ni, Pd, Au
4) FRAME THICKNESS: 0.203mm
5) DIE PAD: 6 X 6mm
6) JEDEC OUTLINE: MO-220
7) DIMENSIONS: MM

PLATING THICKNESS		
Ni	NICKEL	0.50-2.00 μm
Pd	PALLADIUM	0.02-0.15 μm
Au	GOLD	0.003-0.015 μm

TOLERANCE UNLESS NOTED	
X.X	± 0.05
X.XX	± 0.01
X.XXX	± 0.005
X.XXXX	± 0.0005

ALL DIMENSIONS IN
☐INCHES ☐ MILLIMTERS

THIRD ANGLE PROJECTION

APPROVALS		DATE
DRAWN	TST	8/21/10
CHECKED		
ENG		
MFG		
Q.A.		
CUST		
REVISED		

Mirror
Semiconductor™

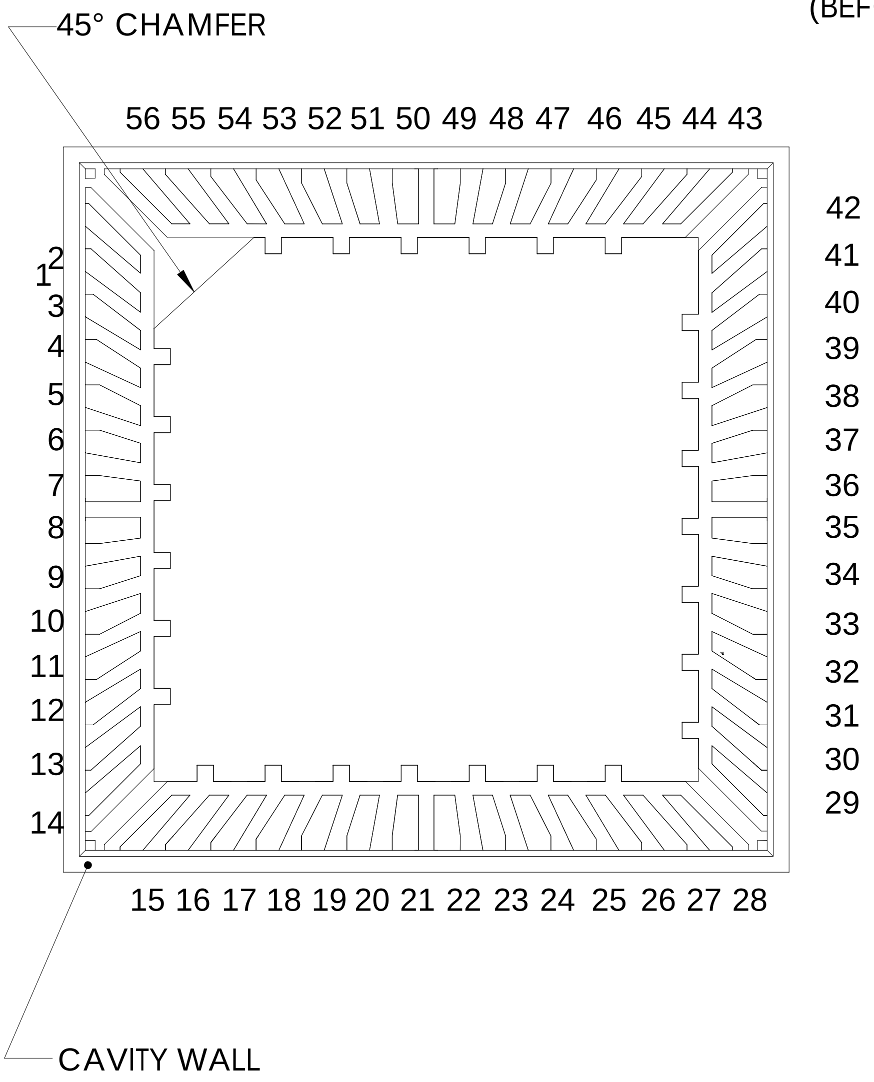
TITLE:
56-LEAD 8mm P=0.5 mm
M-QFN CAVITY PACKAGE

SCALE	SIZE	DWG. NO.	REV
8:1	**A**	**455650** **M-QFN56W.5**	**A**

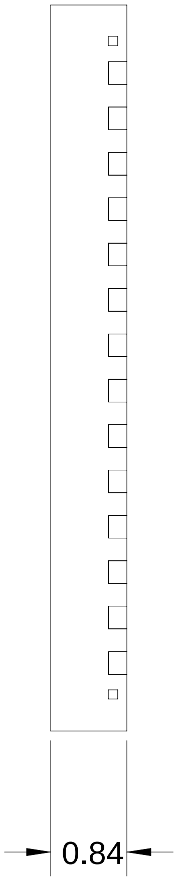
DO NOT SCALE DRAWING | SHEET 1 OF 4

5 4 3 2 1

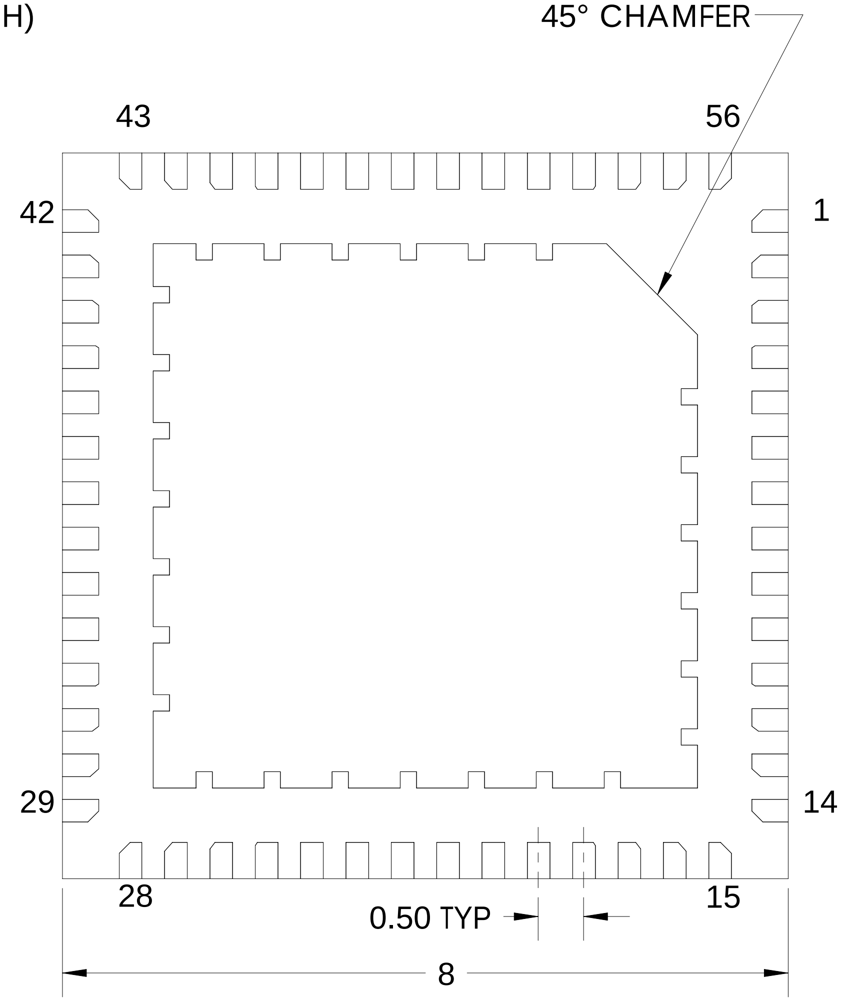
TOP VIEW



SIDE VIEW
(BEFORE LID ATTACH)



BOTTOM VIEW



Mirror
Semiconductor™

TITLE:

56-LEAD 8mm P=0.5 mm
M-QFN CAVITY PACKAGE

SCALE	SIZE	DWG. NO.	REV
12:1	**A**	**455650** **M-QFN56W.5**	**A**

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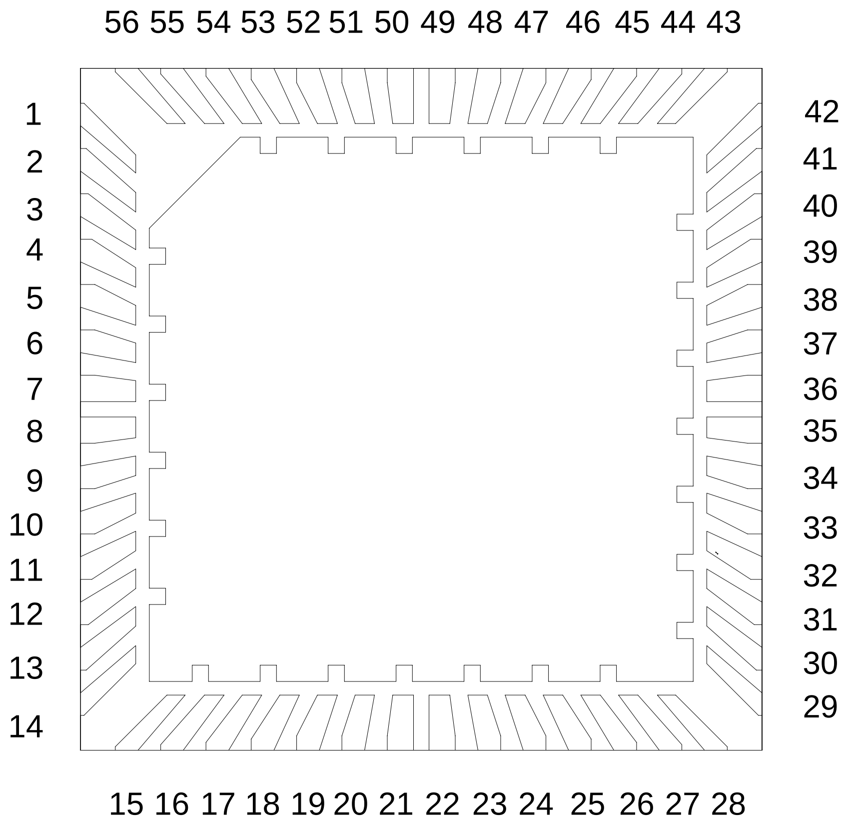
SHEET 2 OF 4

BOND DIAGRAM



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TITLE:

56-LEAD 8mm P=0.5 mm
M-QFN CAVITY PACKAGE

SCALE	SIZE	DWG. NO.	REV
11:1	**A**	**455650** **M-QFN56W.5**	**A**

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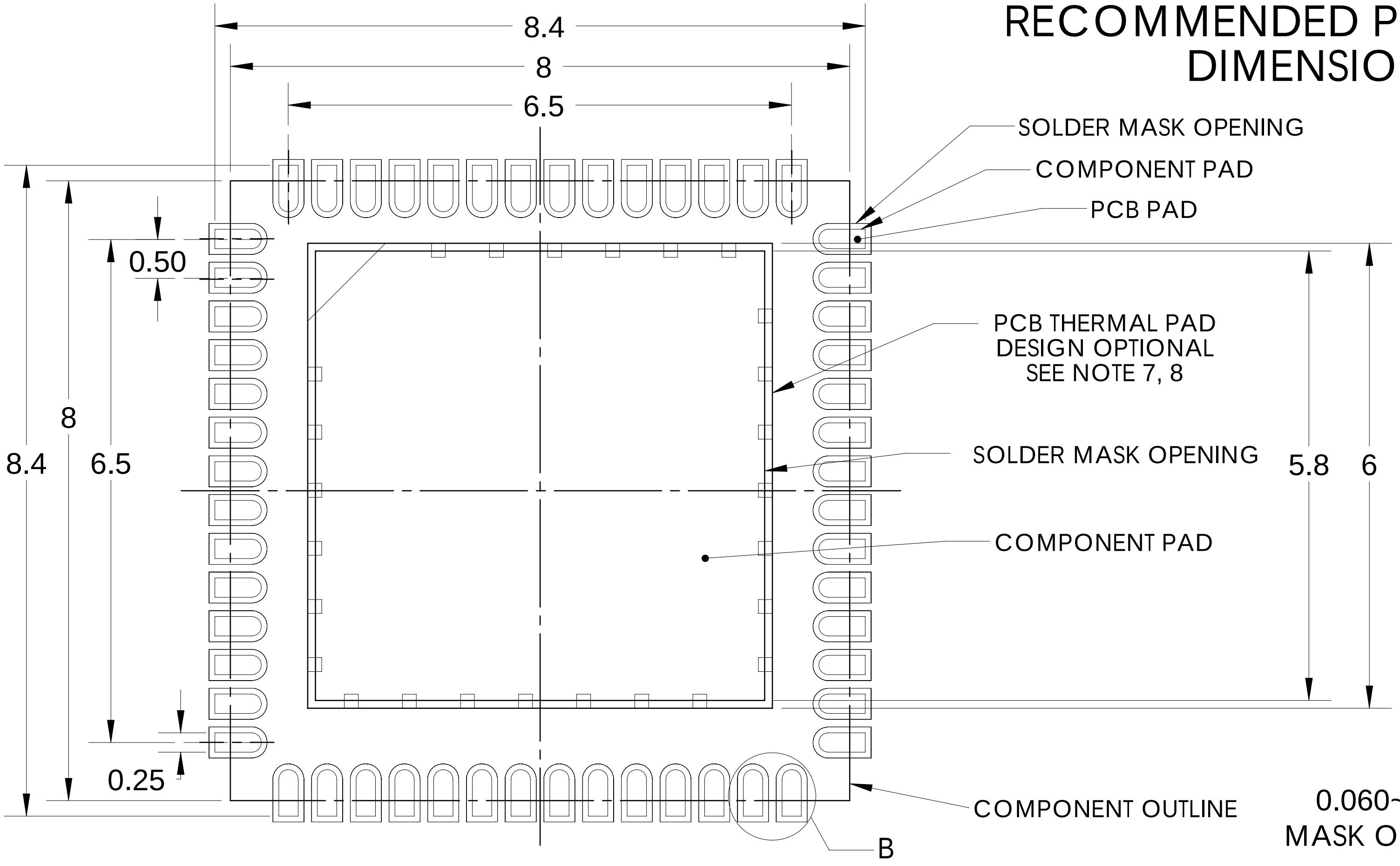
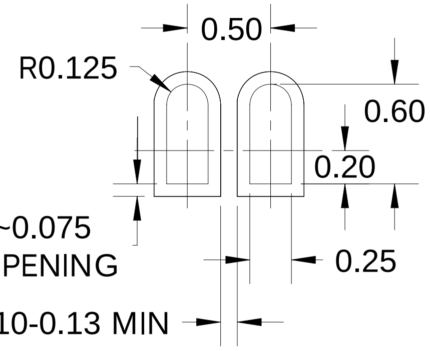
RECOMMENDED PC BOARD LAYOUT
DIMENSIONS IN MM





DETAIL B
SCALE 22 : 1

Notes: (Unless Otherwise Specified).

1) DIMENSIONS ARE PRESENTED ONLY AS A GUIDELINE. DESIGNERS SHOULD USE THEIR OWN KNOWLEDGE BASE WHEN DESIGNING THE PCB.
2) SURROUND EACH SIDE OF I/O PERIMETER PADS WITH 0.060~0.075 mm (NSMD) SOLDER MASK OPENING (2.4~3.0mils). OPTIONALLY OK TO USE RECTANGLE (NSMD) MASK OPENING AROUND I/O PADS.
3) ROUNDED PCB LAND PADS REDUCE SOLDER BRIDGING. PAD CHAMFER ANGLE MAY VARY
4) PCB LANDS SHOULD BE 0.2mm LONGER THAN THE PACKAGE I/O PADS.
5) THE WIDTH OF PERIMETER PCB PADS SHOULD MATCH (1:1) THE SAME WIDTH AS THE PACKAGE PADS.
6) REFER TO INDUSTRY REFERENCES SUCH AS IPC-SM-782 FOR PCB LAND PATTERN DESIGN.
7) THERMAL GROUND PADS MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
   A. MAKE COPPER THERMAL PAD AS LARGE AS POSSIBLE.
   B. DRILL MULTIPLE THERMAL VIAS 0.25~0.33mm DIAMETER USING 0.8~1.2mm PITCH GRID.
   C. PLATE THERMAL VIA BARRELS WITH 1-OUNCE COPPER (18µm).
   D. TENT (COVER) THERMAL VIAS WITH SOLDER MASK 0.1mm LARGER THEN THE VIA DIAMETER.
8) STENCIL DESIGN MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
   A. LASER CUT STENCIL 0.125mm (5mil) THICK. APERTURE SIZE-TO-LAND RATIO OF 1:1.
   B. THE SOLDER PASTE OPENING IN THE THERMAL PAD AREA SHOULD BE A MATRIX ARRAY OF SMALLER APERTURES INSTEAD OF ONE LARGE APERTURE TO CONTROL PASTE AMOUNTS.

C. APPLY 50% TO 80% SOLDER PASTE COVERAGE IN THE THERMAL PAD AREA.

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Semiconductor™

TITLE:
56-LEAD 8mm P=0.5 mm
M-QFN CAVITY PACKAGE

SCALE	SIZE	DWG. NO.	REV
11:1	**A**	**455650** **M-QFN56W.5**	**A**

DO NOT SCALE DRAWING | SHEET 4 OF 4