

- Notes: (Unless Otherwise Specified)
- 1) BODY; PLASTIC, SEMICONDUCTOR GRADE
  - 2) LEAD FRAME: COPPER, C-194F/H
  - 3) LEAD FRAME PLATING: Ni, Pd, Au
  - 4) FRAME THICKNESS: 0.203mm
  - 5) DIE PAD: 10 X 10mm
  - 6) JEDEC OUTLINE: MO-220
  - 7) DIMENSIONS: MM

PLATING THICKNESS		
Ni	NICKEL	0.50-2.00 $\mu\text{m}$
Pd	PALLADIUM	0.02-0.15 $\mu\text{m}$
Au	GOLD	0.003-0.015 $\mu\text{m}$

TOLERANCE UNLESS NOTED		APPROVALS		DATE
X.X	± 0.05	DRAWN	TST	8/21/10
X.XX	± 0.01	<div style="display: flex; align-items: center;"> <div style="margin-right: 10px;"> <input type="checkbox"/> INCHES  <input checked="" type="checkbox"/> MILLIMETERS         </div> <div>           THIRD ANGLE            PROJECTION  </div> </div>		
X.XXX	± 0.005			
X.XXXX	± 0.0005			
ALL DIMENSIONS IN				
		ENG		
		MFG		
		Q.A.		
		CUST		
		REVISED		

**Mirror**  
Semiconductor™

TITLE:  
80-LEAD 12mm P=0.5 mm  
M-QFN CAVITY PACKAGE

SCALE <b>6:1</b>	SIZE <b>A</b>	DWG. NO. <b>458050</b> <b>M-QFN80W.5</b>	REV <b>A</b>
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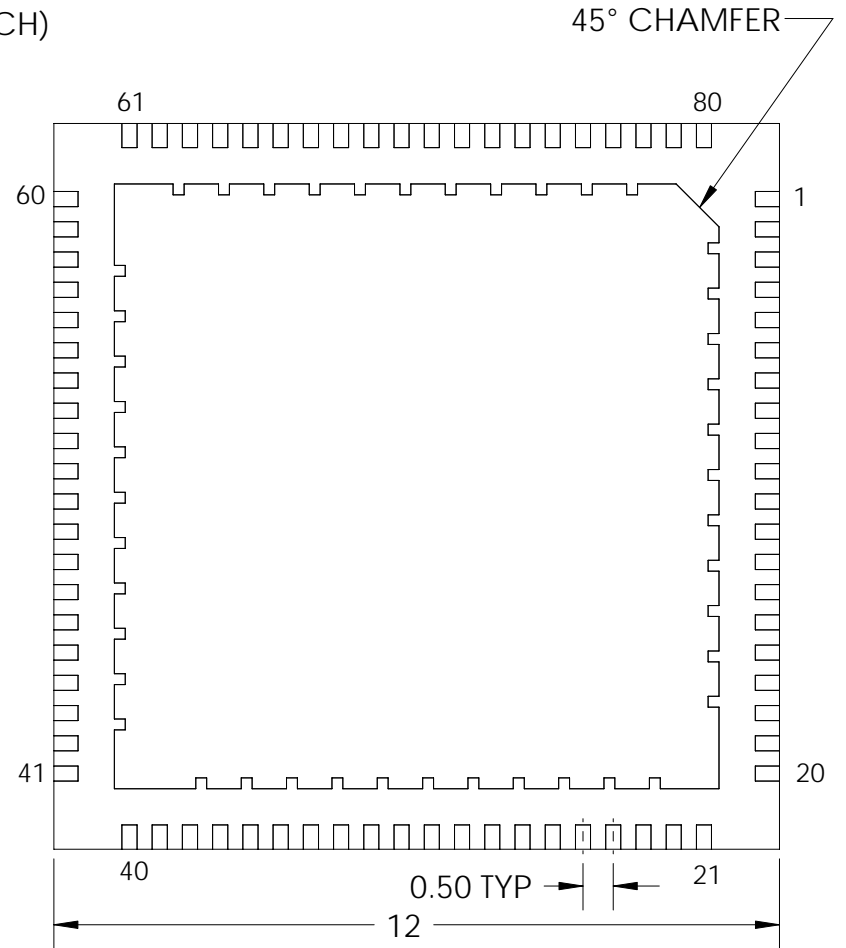
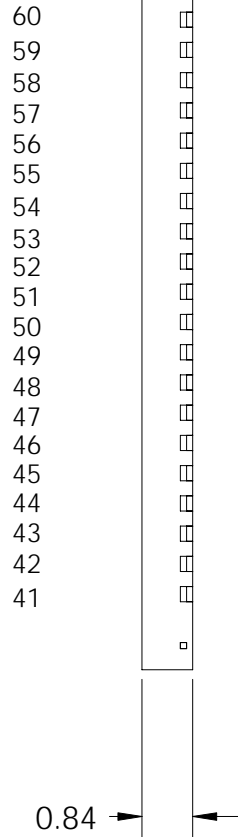
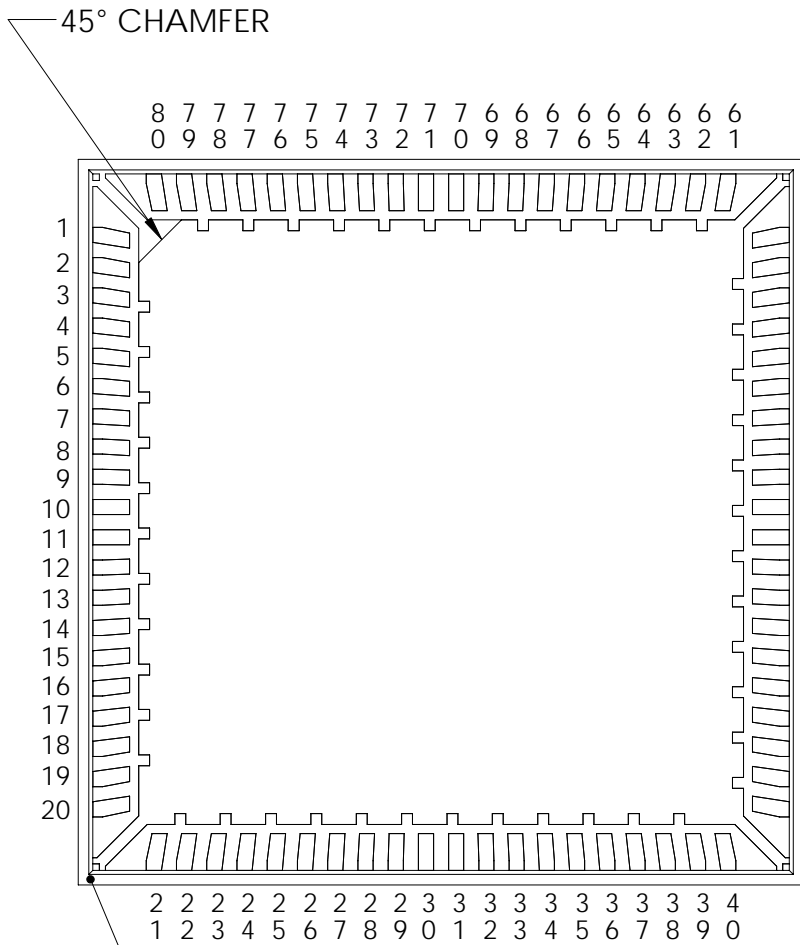
DO NOT SCALE DRAWING      SHEET 1 OF 4

TOP VIEW

PIN LOCATIONS

BOTTOM VIEW

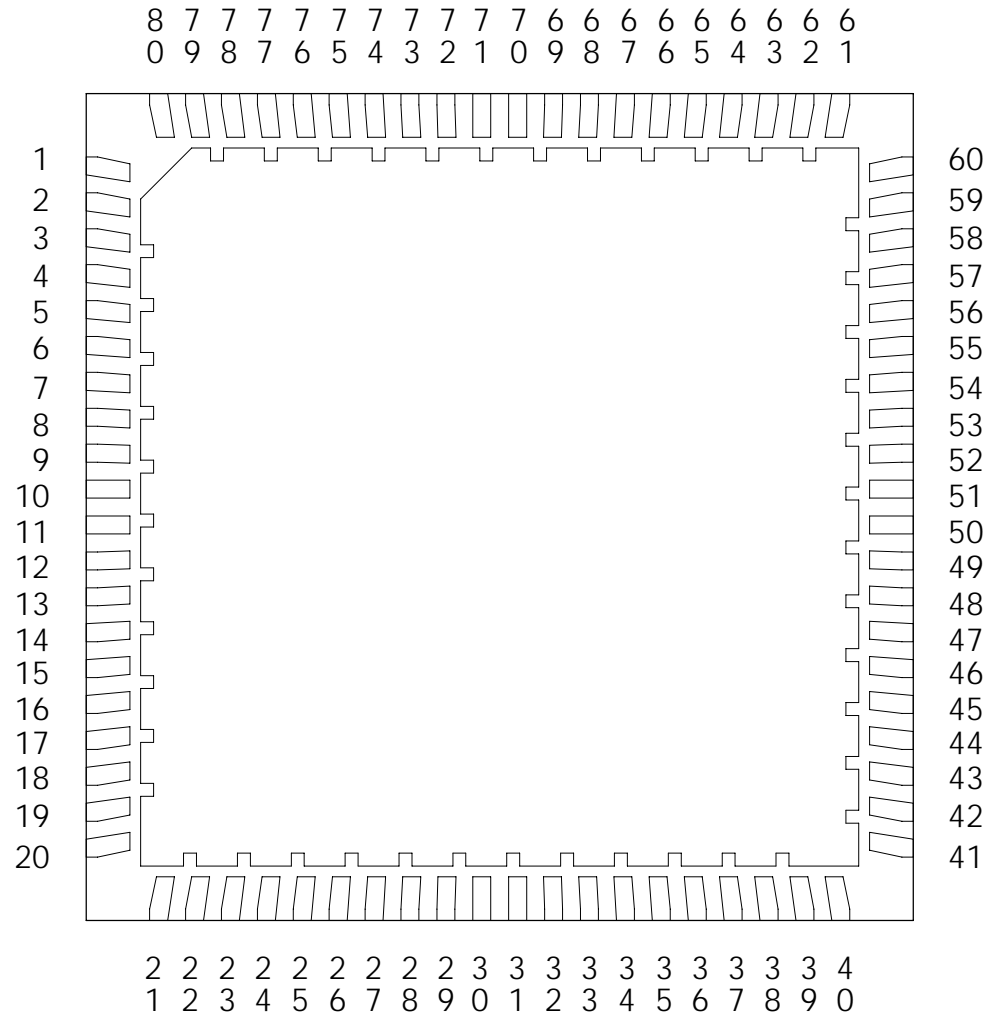
SIDE VIEW  
(BEFORE LID ATTACH)



TITLE:  
80-LEAD 12mm P=0.5 mm  
M-QFN CAVITY PACKAGE

SCALE 8:1	SIZE A	DWG. NO. 458050 M-QFN80W.5	REV A
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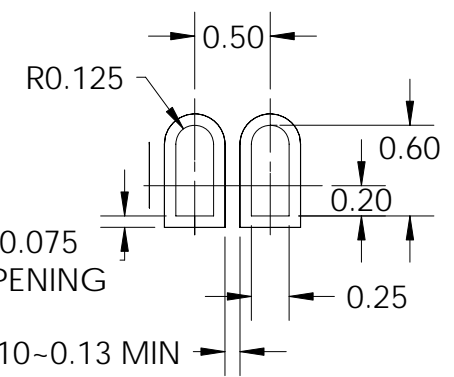
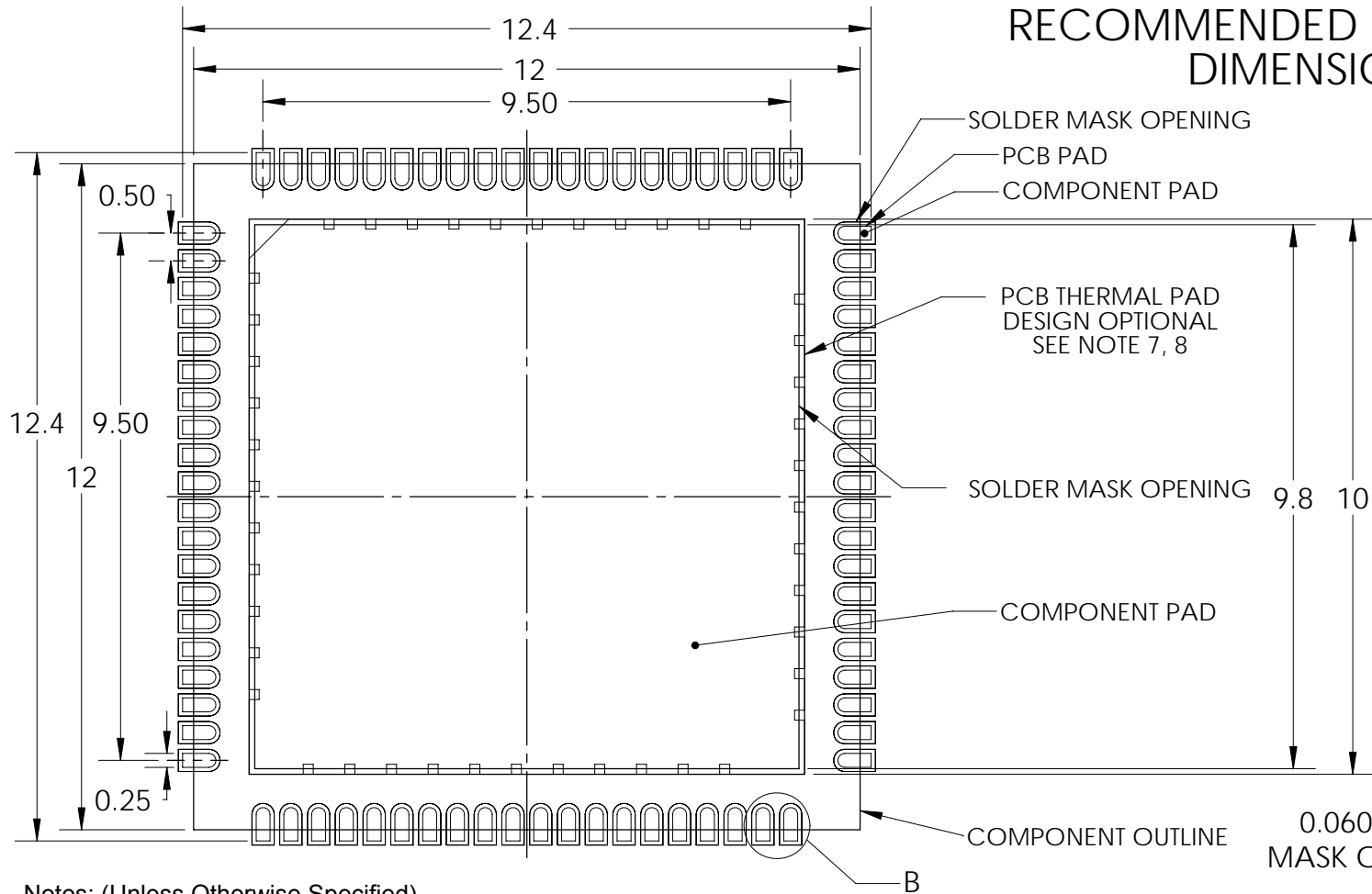
# BOND DIAGRAM



TITLE:  
 80-LEAD 12mm P=0.5 mm  
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SCALE	SIZE	DWG. NO.	REV
9.5:1	A	458050 M-QFN80W.5	A

# RECOMMENDED PC BOARD LAYOUT DIMENSIONS IN MM



DETAIL B  
SCALE 20 : 1

**Notes: (Unless Otherwise Specified).**

- 1) DIMENSIONS ARE PRESENTED ONLY AS A GUIDELINE. DESIGNERS SHOULD USE THEIR OWN KNOWLEDGE BASE WHEN DESIGNING THE PCB.
- 2) SURROUND EACH SIDE OF I/O PERIMETER PADS WITH 0.060~0.075 mm (NSMD) SOLDER MASK OPENING (2.4~3.0mils). OPTIONALLY OK TO USE RECTANGLE (NSMD) MASK OPENING AROUND I/O PADS.
- 3) ROUNDED PCB LAND PADS REDUCE SOLDER BRIDGING. PAD CHAMFER ANGLE MAY VARY
- 4) PCB LANDS SHOULD BE 0.2mm LONGER THAN THE PACKAGE I/O PADS.
- 5) THE WIDTH OF PERIMETER PCB PADS SHOULD MATCH (1:1) THE SAME WIDTH AS THE PACKAGE PADS.
- 6) REFER TO INDUSTRY REFERENCES SUCH AS IPC-SM-782 FOR PCB LAND PATTERN DESIGN.
- 7) THERMAL GROUND PADS MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
  - A. MAKE COPPER THERMAL PAD AS LARGE AS POSSIBLE.
  - B. DRILL MULTIPLE THERMAL VIAS 0.25~0.33mm DIAMETER USING 0.8~1.2mm PITCH GRID.
  - C. PLATE THERMAL VIA BARRELS WITH 1-OUNCE COPPER (18µm).
  - D. TENT (COVER) THERMAL VIAS WITH SOLDER MASK 0.1mm LARGER THEN THE VIA DIAMETER.
- 8) STENCIL DESIGN MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
  - A. LASER CUT STENCIL 0.125mm (5mil) THICK. APERTURE SIZE-TO-LAND RATIO OF 1:1.
  - B. THE SOLDER PASTE OPENING IN THE THERMAL PAD AREA SHOULD BE A MATRIX ARRAY OF SMALLER APERTURES INSTEAD OF ONE LARGE APERTURE TO CONTROL PASTE AMOUNTS.
  - C. APPLY 50% TO 80% SOLDER PASTE COVERAGE IN THE THERMAL PAD AREA.



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