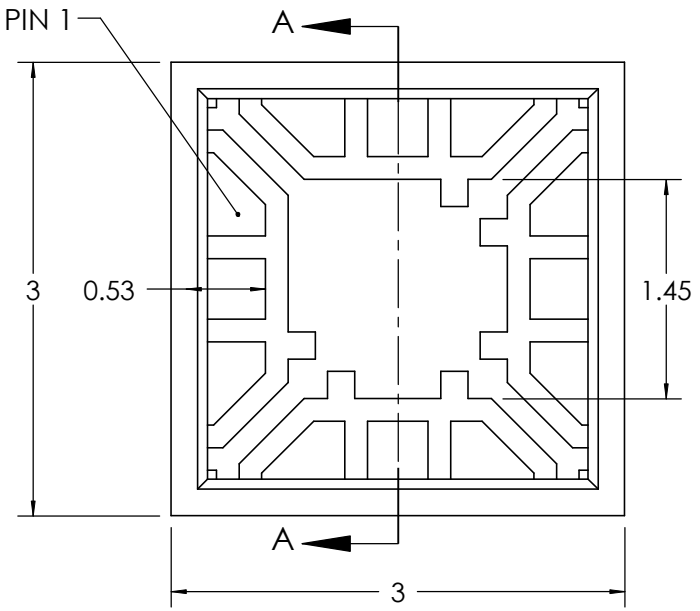
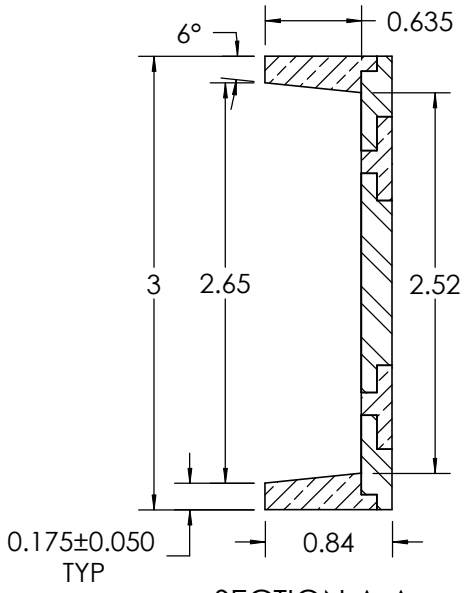
TOP VIEW

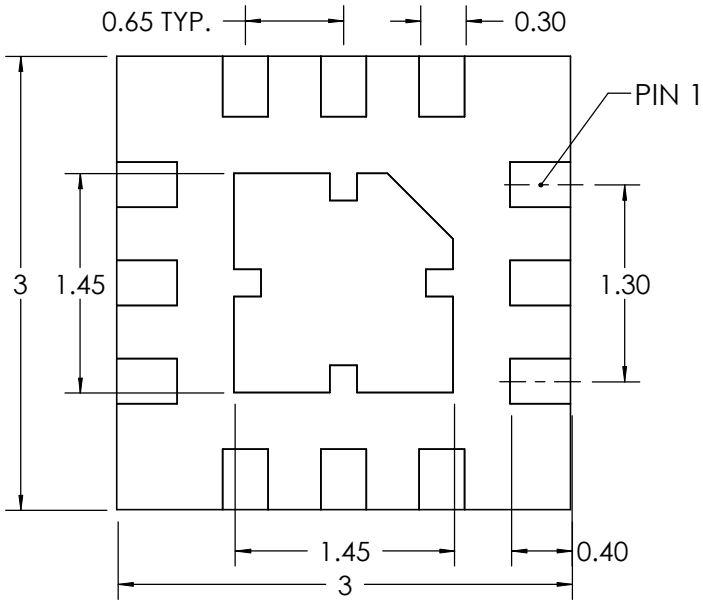


SIDE VIEW

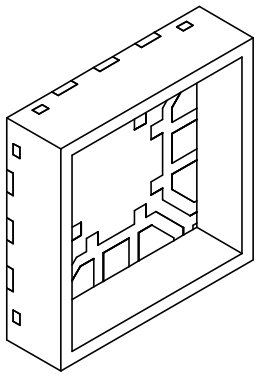


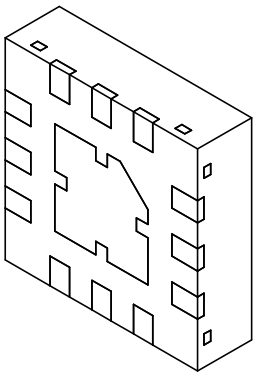
SECTION A-A

BOTTOM VIEW



Notes: (Unless Otherwise Specified)
1) BODY; PLASTIC, SEMICONDUCTOR GRADE
2) LEAD FRAME: COPPER, C-194F/H
3) LEAD FRAME PLATING: Ni, Pd, Au
4) FRAME THICKNESS: 0.203mm
5) DIE PAD: 1.45 X 1.45mm
6) JEDEC OUTLINE: MO-220





TOLERANCES UNLESS NOTED	
X.X	± 0.05
X.XX	± 0.01
X.XXX	± 0.005
X.XXXX	± 0.0005

ALL DIMENSIONS IN

☐ INCHES ☒ MILLIMETERS

THIRD ANGLE PROJECTION

APPROVALS		DATE
DRAWN	EDK	2/15/2012
CHECKED		
ENG APPR.		
MFG APPR.		
Q.A.		
CUST.		
REVISED		

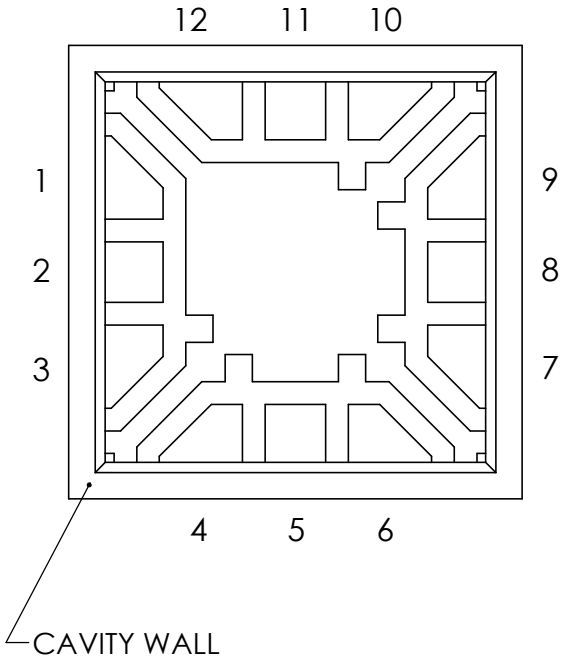
Mirror Semiconductor
www.MirrorSemi.com

TITLE: **M-QFN12W.65-3MM**
12-LEAD 3mm P=0.65 mm
QFN CAVITY PACKAGE

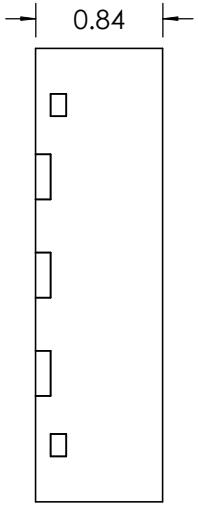
SCALE	SIZE	DWG. NO.	REV
20:1	A	461370	A

DO NOT SCALE DRAWING | SHEET 1 OF 4

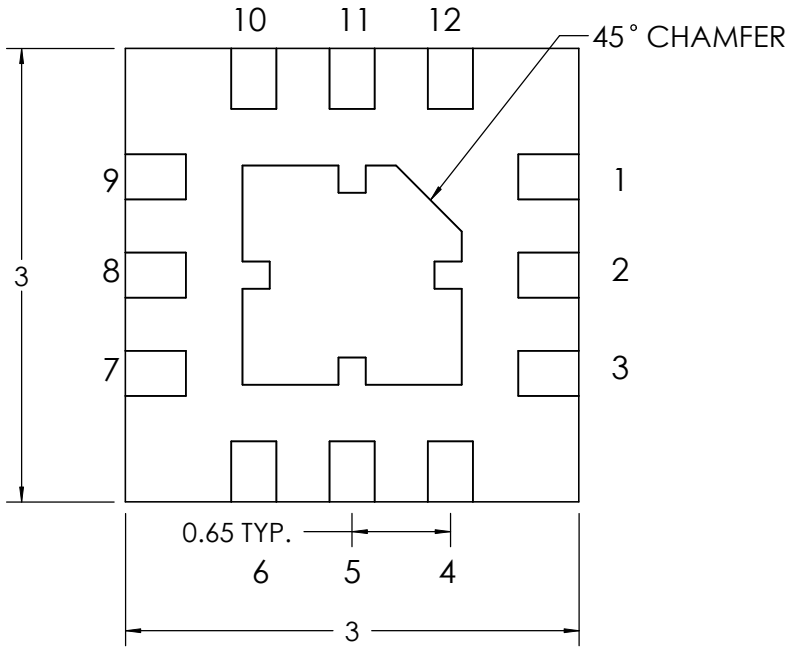
TOP VIEW



SIDE VIEW
(BEFORE LID ATTACH)

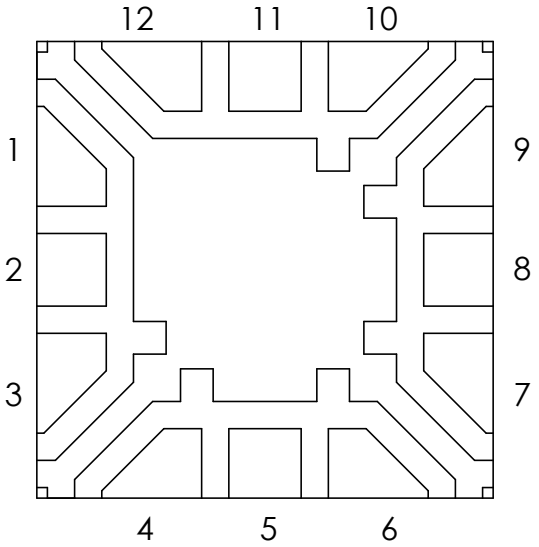


BOTTOM VIEW

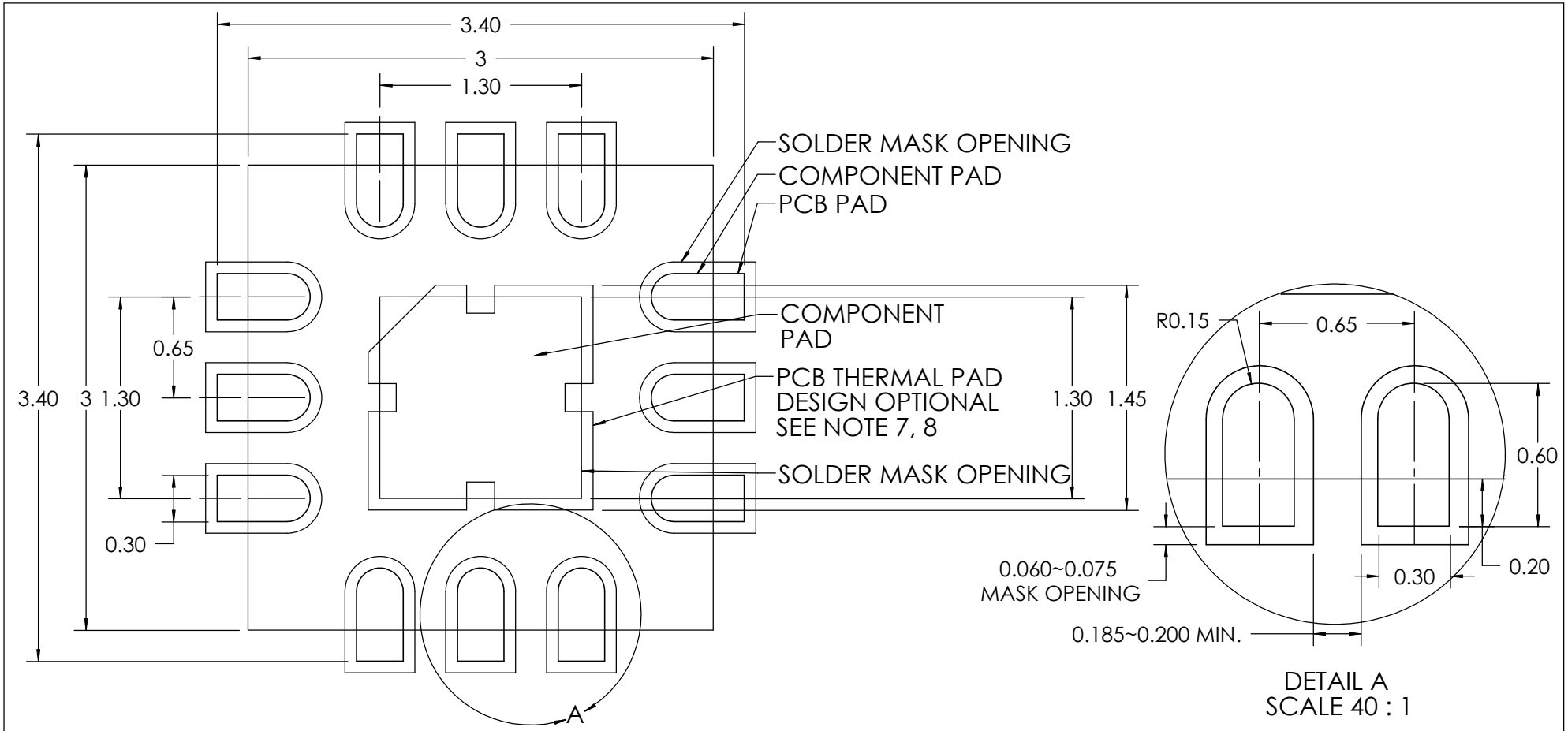


Mirror Semiconductor www.MirrorSemi.com			
TITLE: **M-QFN12W.65-3MM** 12-LEAD 3mm P=0.65 mm QFN CAVITY PACKAGE LEAD NUMBERING			
SCALE **20:1**	SIZE **A**	DWG. NO. **461370**	REV A
DO NOT SCALE DRAWING			SHEET 2 OF 4

BOND DIAGRAM



Mirror Semiconductor www.MirrorSemi.com			
TITLE: **M-QFN12W.65-3MM** 12-LEAD 3mm P=0.65 mm QFN CAVITY PACKAGE BOND DIAGRAM			
SCALE **24:1**	SIZE **A**	DWG. NO. **461370**	REV A
DO NOT SCALE DRAWING		SHEET 3 OF 4	



DETAIL A
SCALE 40 : 1

Notes: (Unless Otherwise Specified).

1. DIMENSIONS ARE PRESENTED ONLY AS A GUIDELINE. DESIGNERS SHOULD USE THEIR OWN KNOWLEDGE BASE WHEN DESIGNING THE PCB.
2. SURROUND EACH SIDE OF I/O PERIMETER PADS WITH 0.060~0.075 mm (2.4~3.0mils) NSMD SOLDER MASK OPENING. OPTIONALLY OK TO USE RECTANGLE (NSMD) MASK OPENING AROUND I/O PADS.
3. ROUNDED PCB LAND PADS REDUCE SOLDER BRIDGING. PAD CHAMFER ANGLE MAY VARY.
4. PCB LANDS SHOULD BE 0.2mm LONGER THAN THE PACKAGE I/O PADS.
5. THE WIDTH OF PERIMETER PCB PADS SHOULD MATCH (1:1) THE WIDTH OF THE PACKAGE PADS.
6. REFER TO INDUSTRY REFERENCES SUCH AS IPC-SM-782 FOR PCB LAND PATTERN DESIGN.
7. THERMAL GROUND PADS MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
   A. MAKE COPPER THERMAL PAD AS LARGE AS POSSIBLE.
   B. DRILL MULTIPLE THERMAL VIAS 0.25~0.33mm DIAMETER USING 0.8~1.2mm PITCH GRID.
   C. PLATE THERMAL VIA BARRELS WITH 1-OUNCE COPPER (18µm).
   D. TENT (COVER) THERMAL VIAS WITH SOLDER MASK 0.1mm LARGER THAN THE VIA DIAMETER.
8. STENCIL DESIGN MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
   A. LASER CUT STENCIL 0.125mm (5mil) THICK. APERTURE SIZE-TO-LAND RATIO OF 1:1.
   B. THE SOLDER PASTE OPENING IN THE THERMAL PAD AREA SHOULD BE A MATRIX ARRAY OF SMALLER APERATURES INSTEAD OF ONE LARGE APERATURE TO CONTROL PASTE AMOUNTS.
   C. APPLY 50% TO 80% SOLDER PASTE COVERAGE IN THE PAD AREA.

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TITLE: 12-LEAD 3mm P=0.65 mm QFN CAVITY PACKAGE RECOMMENDED PCB LAYOUT

SCALE	SIZE	DWG. NO.	REV
26:1	A	461370	A

DO NOT SCALE DRAWING | SHEET 4 OF 4