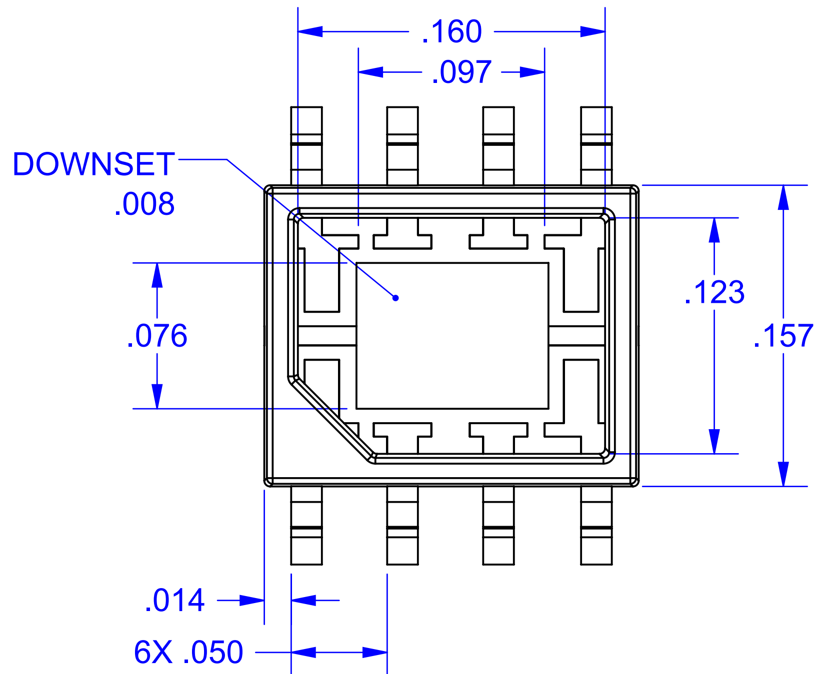
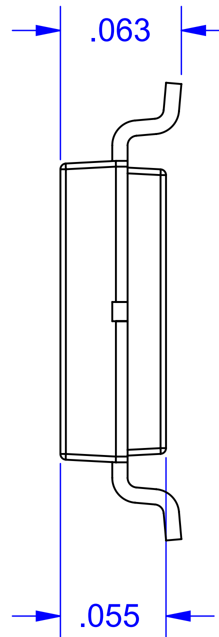
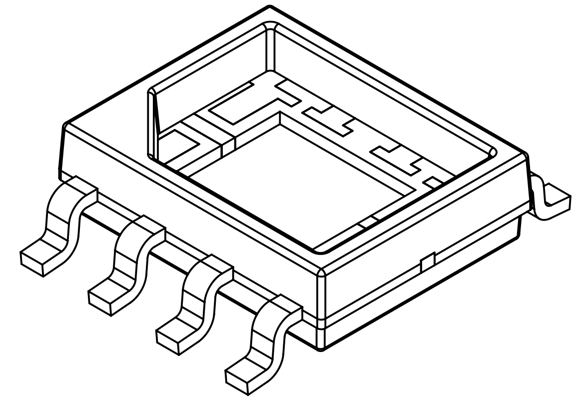
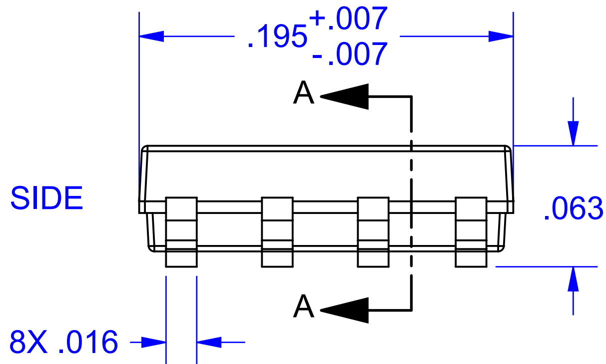
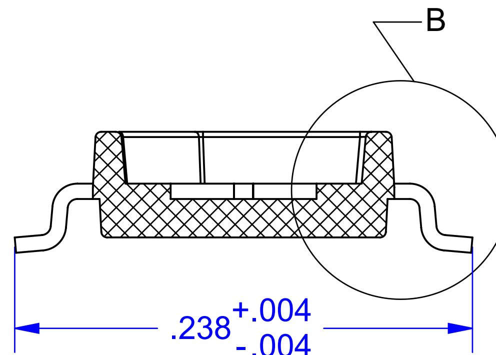
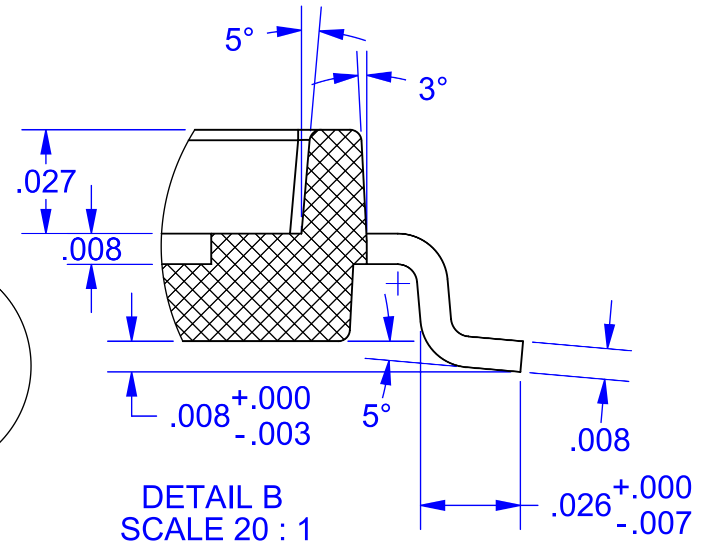




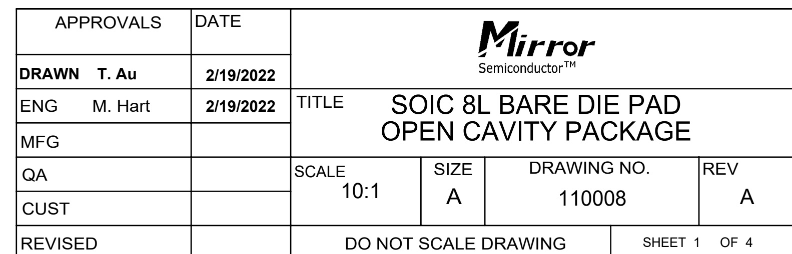






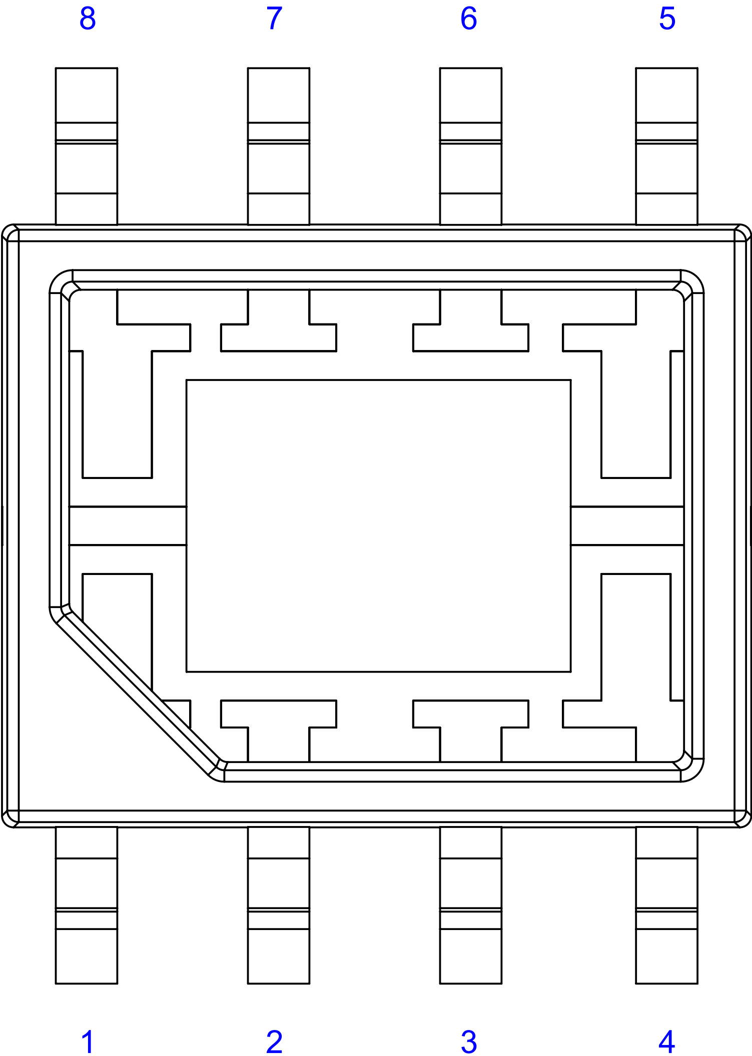


Notes: (Unless Otherwise Specified).
1) DIMENSIONS: INCHES [MM].
2) PACKAGE CONFORMS TO JEDEC MS-012.
3) BODY: SEMICONDUCTOR GRADE MOLDING EPOXY.
4) LEAD FRAME: COPPER ALLOY A194 FULL HARD.
5) PLATING: NICKEL 100~300 MICROINCHES (2.5~7.6μM)THICK.
GOLD PLATE PER MIL-G-45204, TYPE 3, GRADE A, CLASS 1.



APPROVALS	DATE	Mirror Semiconductor™			
DRAWN T. Au	2/19/2022				
ENG M. Hart	2/19/2022	TITLE SOIC 8L BARE DIE PAD OPEN CAVITY PACKAGE			
MFG					
QA		SCALE 10:1	SIZE A	DRAWING NO. 110008	REV A
CUST					
REVISED		DO NOT SCALE DRAWING		SHEET 1 OF 4	

BOND DIAGRAM



NOTES:

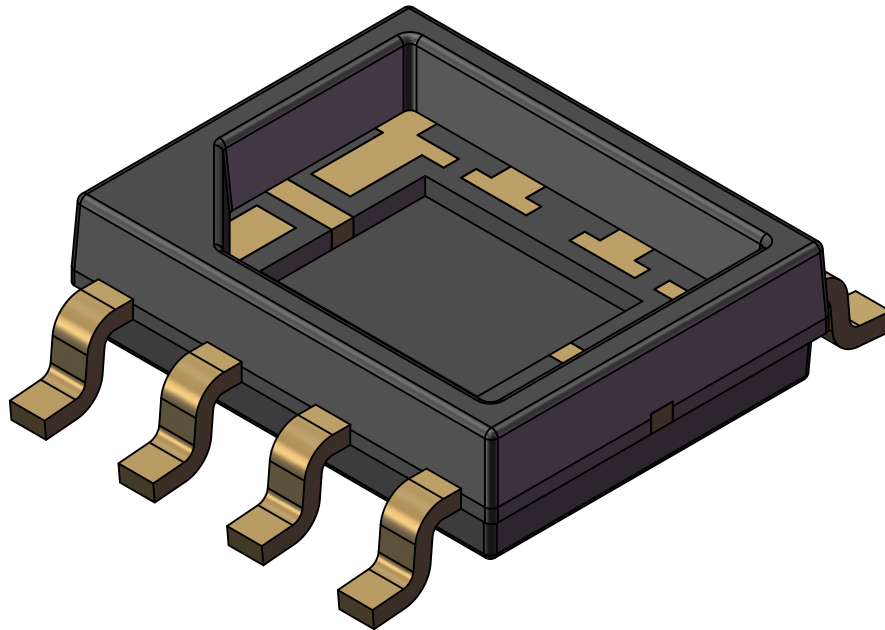
1. BARE DIE PAD AREA (WITHOUT METALLIZATION).
2. DIE PAD AREA: 0.076 x 0.097-INCH (1.9 x 2.5mm).
3. DOWNSET: 0.008-INCH (0.20mm).

Mirror Semiconductor™

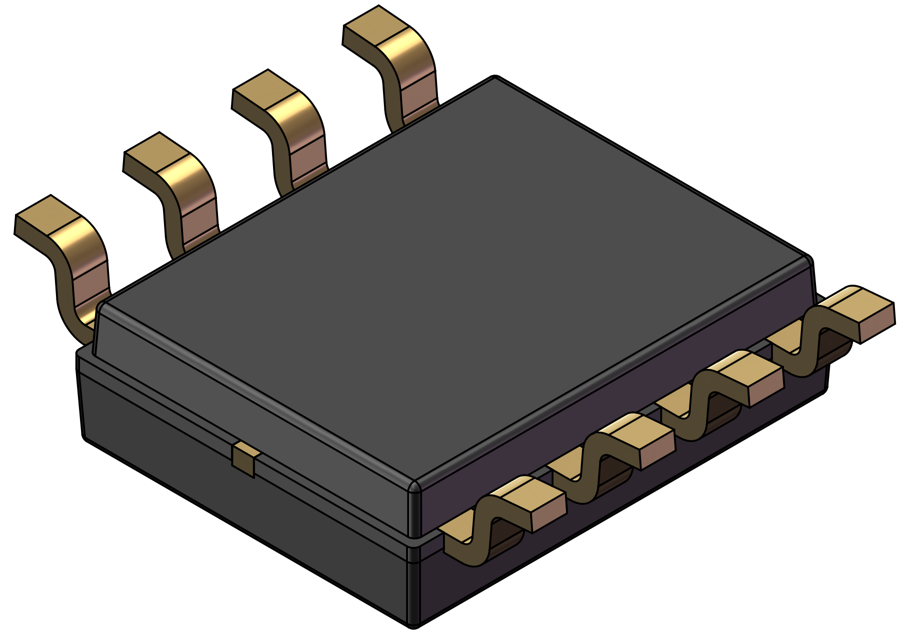
TITLE	SOIC 8L BARE DIE PAD OPEN CAVITY PACKAGE		
SCALE 20:1	SIZE A	DRAWING NO. 110008	REV A
DO NOT SCALE DRAWING		SHEET 2 OF 4	

MODEL

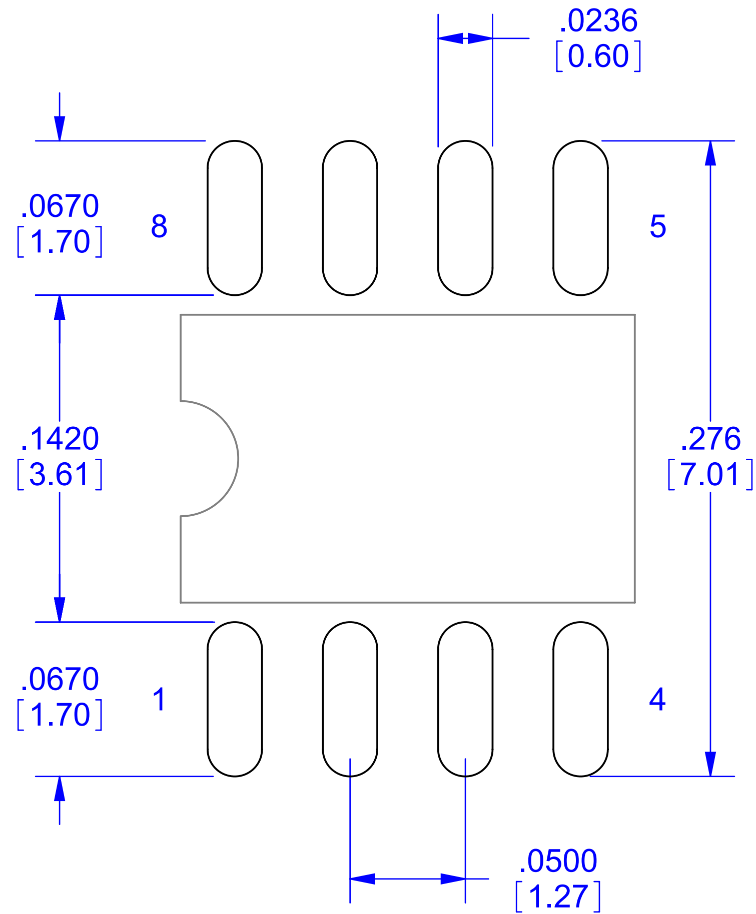
TOP



BOTTOM



TITLE	SOIC 8L BARE DIE PAD OPEN CAVITY PACKAGE		
SCALE 16:1	SIZE A	DRAWING NO. 110008	REV A
DO NOT SCALE DRAWING		SHEET 3 OF 4	



NOTES:
1. DIMENSIONS INCH [mm].

Mirror Semiconductor™			
TITLE	SOIC 8L BARE DIE PAD OPEN CAVITY PACKAGE		
SCALE 12:1	SIZE A	DRAWING NO. 110008	REV A
DO NOT SCALE DRAWING		SHEET 4 OF 4	