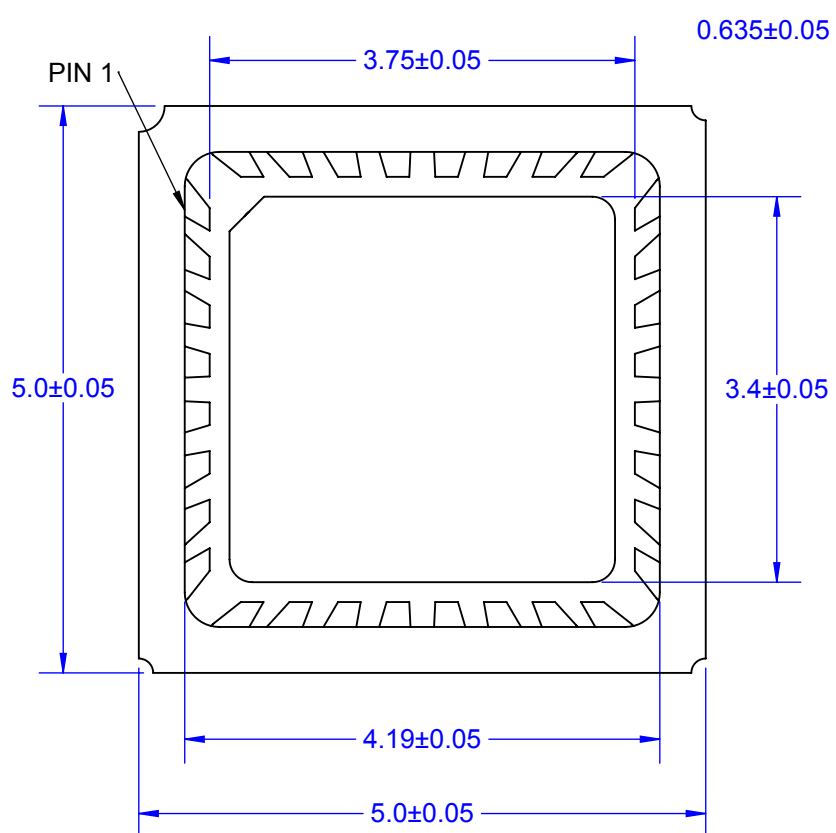
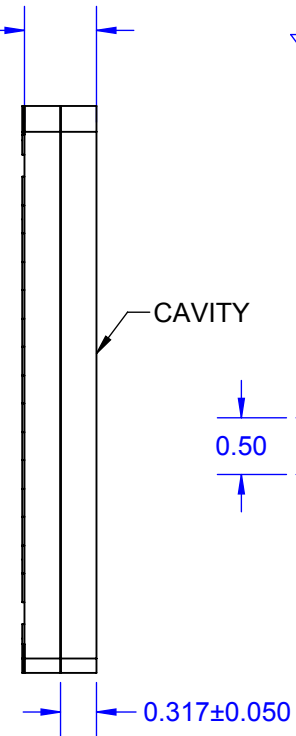


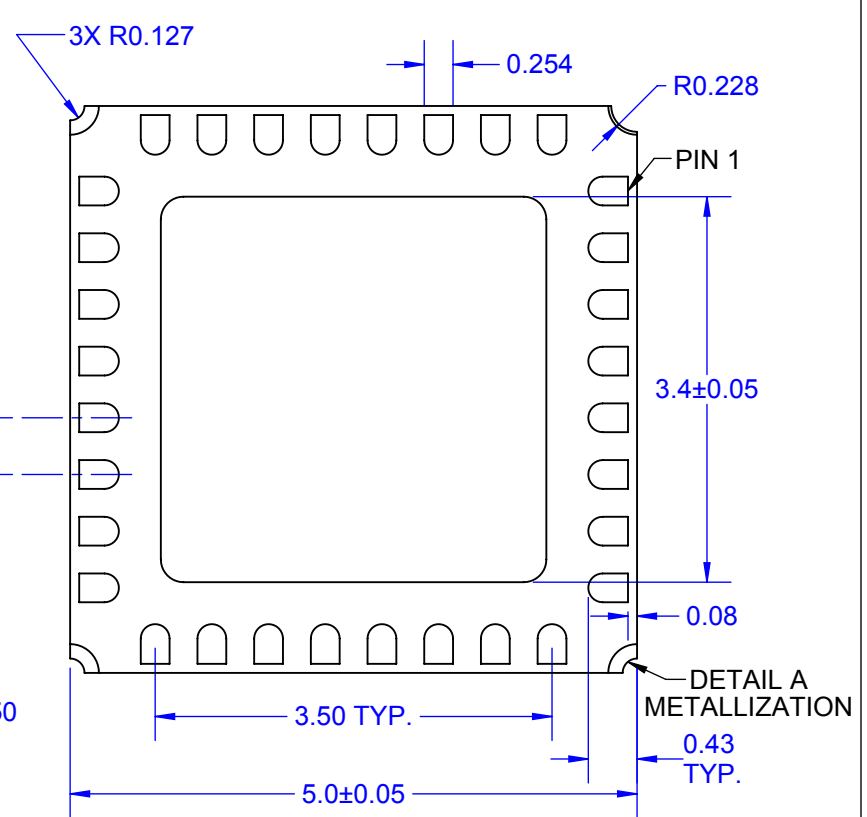
**TOP VIEW**



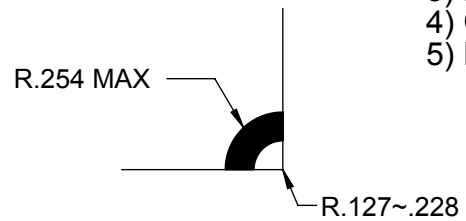
**SIDE VIEW**



**BOTTOM VIEW**



**DETAIL A  
METALLIZATION  
4 CORNERS**

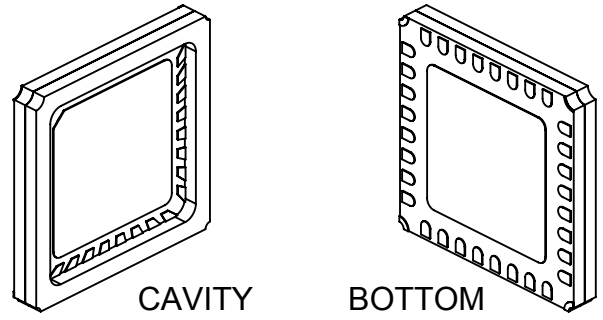


ACTUAL SHAPE OF CORNER PADS MAY VARY

**Notes:**

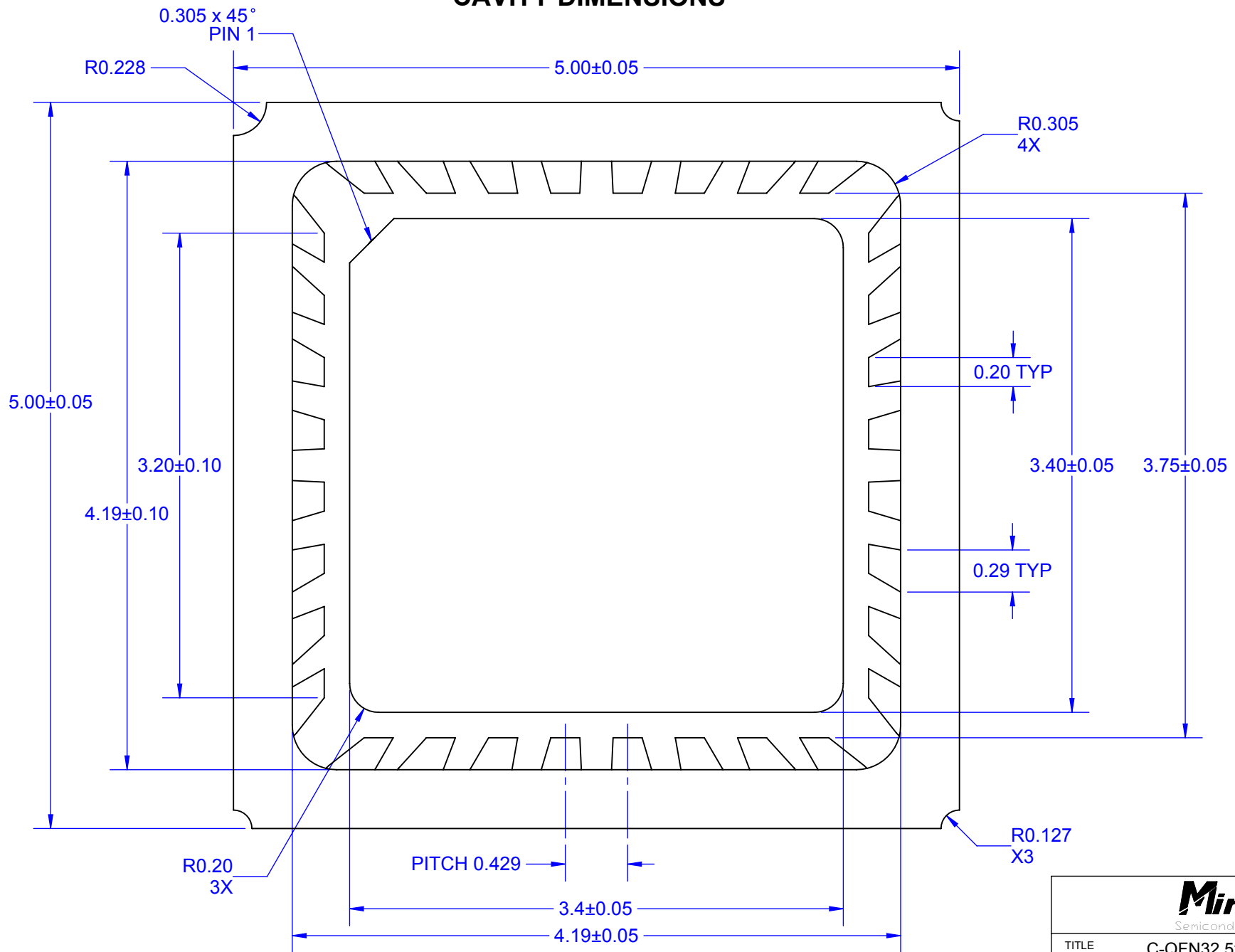
- 1) BODY: CERAMIC Alumina Al<sub>2</sub>O<sub>3</sub> WHITE. 94% MIN
- 2) PADS: Ni 1.27um (MIN). Au 0.76~1.5um.
- 3) BASE METAL TUNGSTEN.
- 4) CAVITY DEPTH 0.317 ±0.050.
- 5) LID: CERAMIC Alumina BLACK (WHITE OPTIONAL).

**MODEL**



APPROVALS	DATE	<b>Mirror</b> Semiconductor™			
DRAWN T.Au	09/27/14				
ENG M. Hart	09/27/14	TITLE C-QFN32L 5x5 P.5mm OUTLINE			
MFG		SCALE	SIZE	DRAWING NO.	REV
QA		15:1	A	353230	A
CUST		DO NOT SCALE DRAWING			SHEET 1 OF 6
REVISED					

# CAVITY DIMENSIONS



**Mirror**  
Semiconductor™

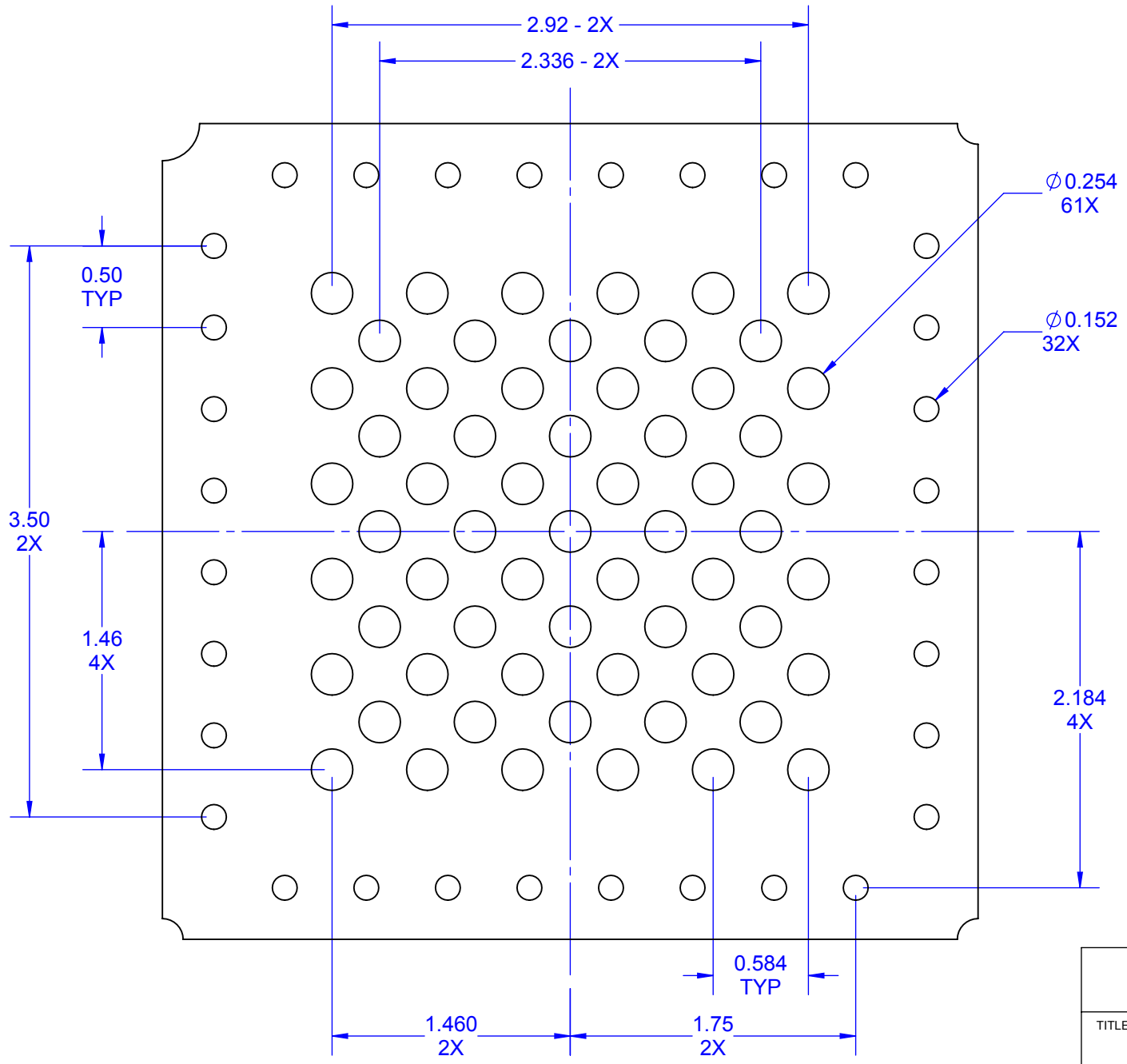
TITLE C-QFN32 5x5 P.5mm  
BONDING DIAGRAM

SCALE 27:1	SIZE A	DRAWING NO. 353230	REV A
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DO NOT SCALE DRAWING

SHEET 2 OF 6

# VIA DETAIL LAYER

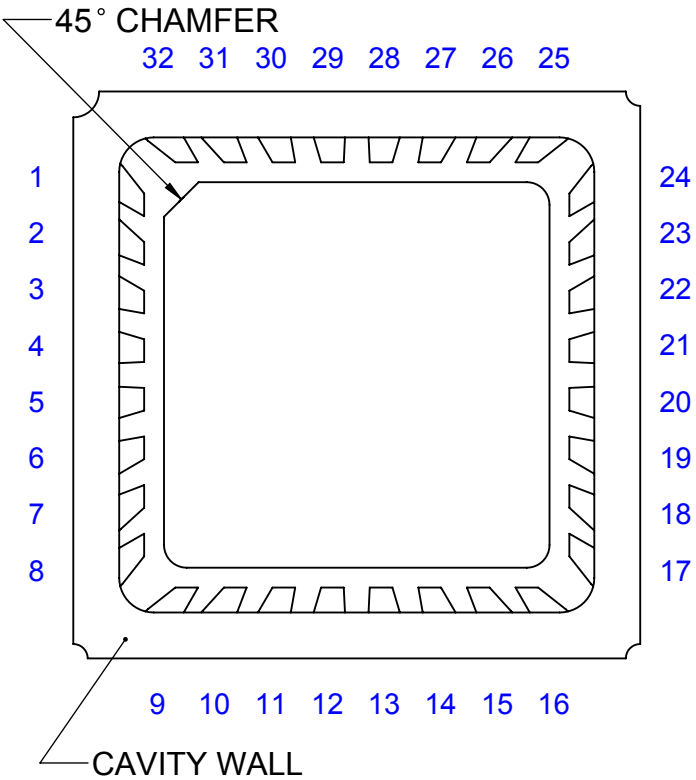


NOTE: VIAS ARE PLUGGED AND CAPPED ON TOP AND BOTTOM.

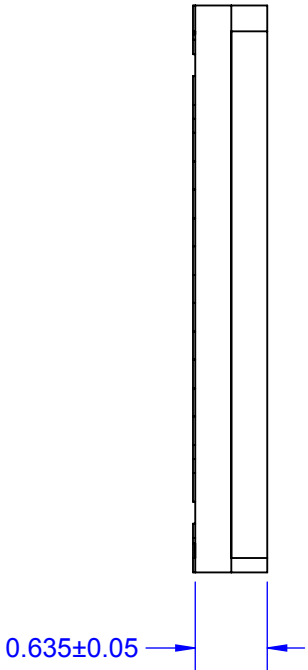
<b>Mirror</b> Semiconductor™			
TITLE C-QFN 32L 5x5 P.5mm CERAMIC CAVITY PACKAGE			
SCALE 27:1	SIZE A	DRAWING NO. 353230	REV A
DO NOT SCALE DRAWING			SHEET 3 OF 6

# PIN LOCATIONS

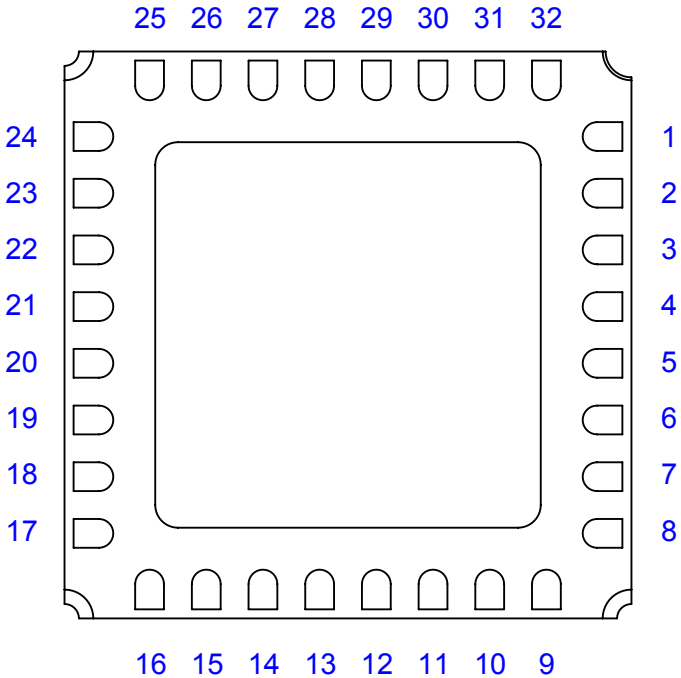
TOP VIEW



SIDE VIEW



BOTTOM VIEW



TITLE C-QFN 32L 5x5 P.5mm CERAMIC CAVITY PACKAGE			
SCALE	SIZE	DRAWING NO.	REV
15:1	A	353230	A
DO NOT SCALE DRAWING			SHEET 4 OF 6

# BONDING DIAGRAM

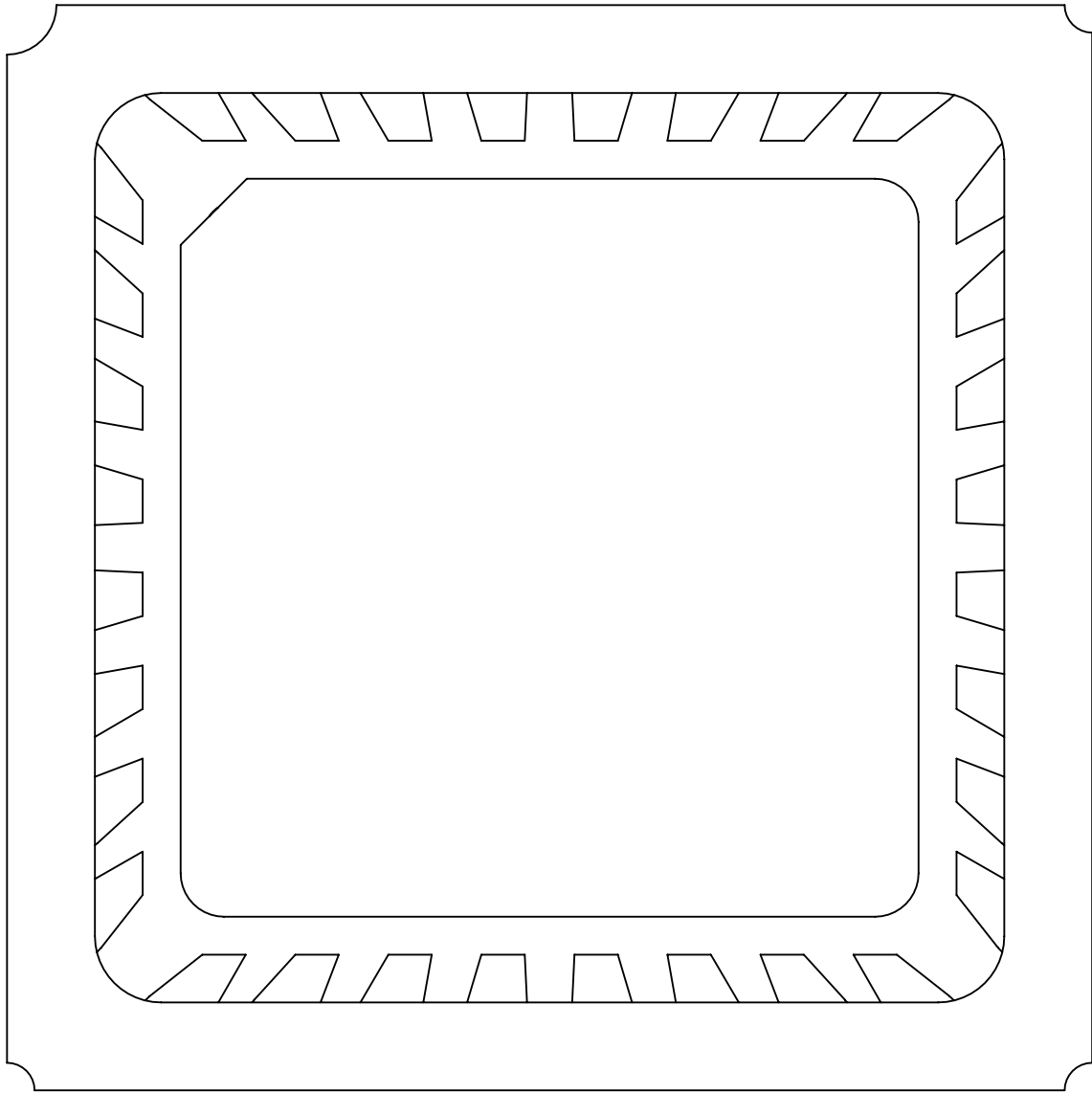
PIN 1  
CHAMFER

32 31 30 29 28 27 26 25

1  
2  
3  
4  
5  
6  
7  
8

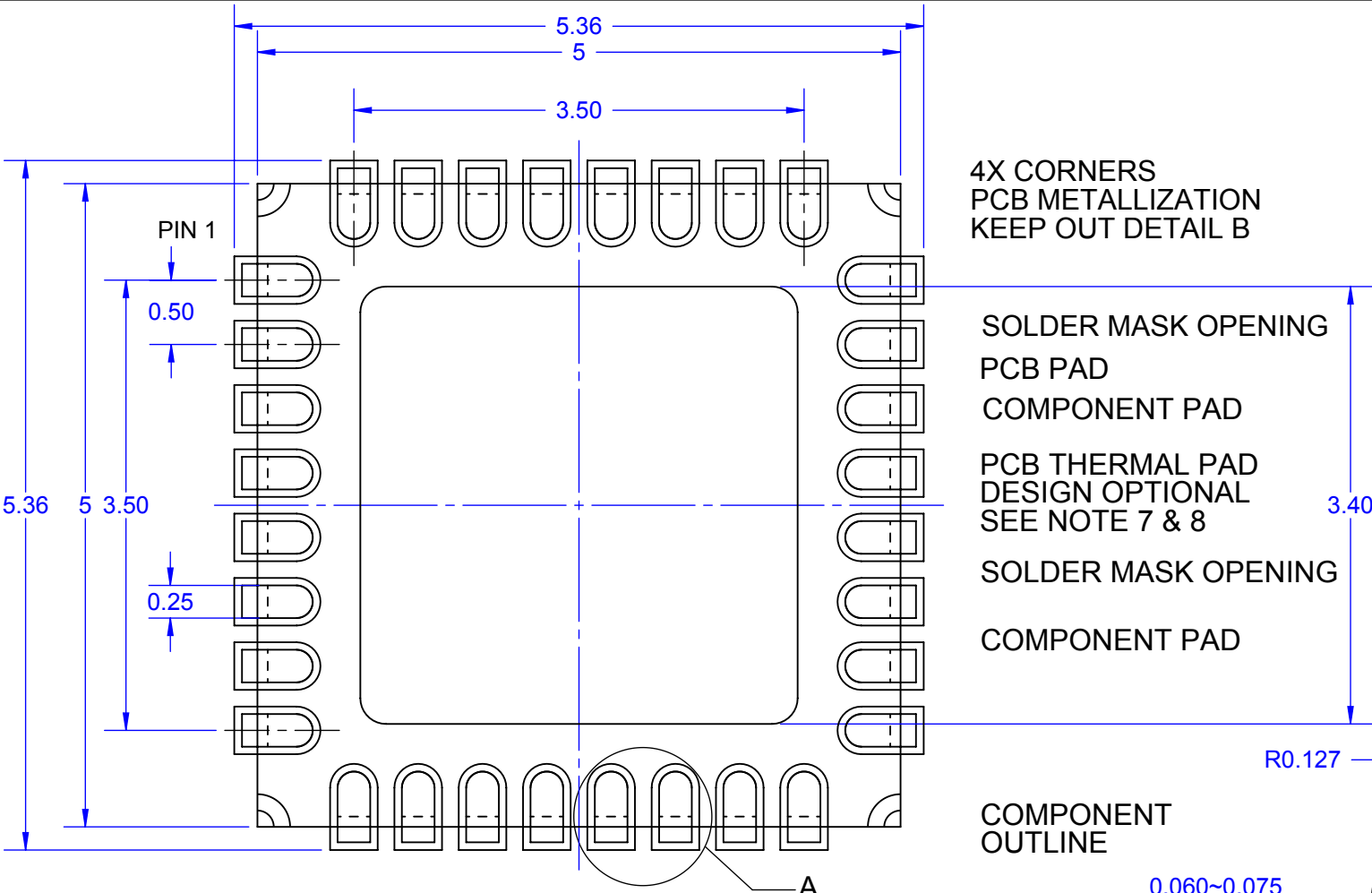
24  
23  
22  
21  
20  
19  
18  
17

9 10 11 12 13 14 15 16



TITLE			
C-QFN 32L 5x5 P.5mm CERAMIC CAVITY PACKAGE			
SCALE	SIZE	DRAWING NO.	REV
30:1	A	353230	A
DO NOT SCALE DRAWING			SHEET 5 OF 6

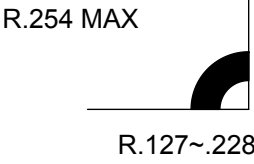
# PC BOARD LAYOUT DIMENSIONS IN MM VIEW FROM TOP



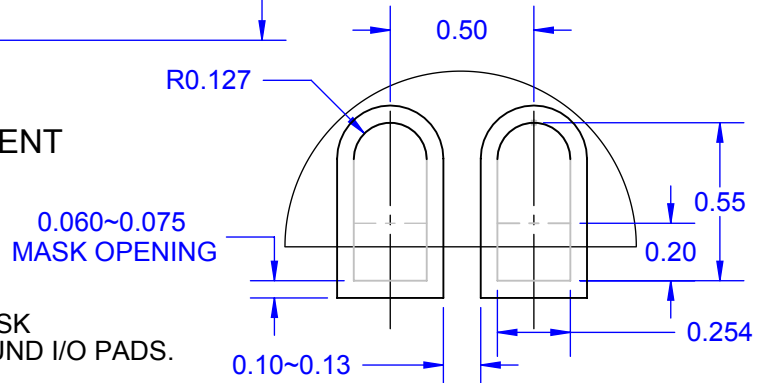
4X CORNERS  
PCB METALLIZATION  
KEEP OUT DETAIL B

SOLDER MASK OPENING  
PCB PAD  
COMPONENT PAD  
PCB THERMAL PAD  
DESIGN OPTIONAL  
SEE NOTE 7 & 8  
SOLDER MASK OPENING  
COMPONENT PAD

DETAIL B  
AVOID METAL ON  
PCB IN CORNERS



COMPONENT  
OUTLINE



DETAIL A  
SCALE 40:1

Notes: (Unless Otherwise Specified).

- 1) DIMENSIONS ARE PRESENTED ONLY AS A GUIDELINE. DESIGNERS SHOULD USE THEIR OWN KNOWLEDGE BASE WHEN DESIGNING THE PCB.
- 2) SURROUND EACH SIDE OF I/O PERIMETER PADS WITH 0.060~0.075 mm (NSMD) SOLDER MASK OPENING (2.4~3.0mils) OPTIONALLY OK TO USE RECTANGLE (NSMD) MASK OPENING AROUND I/O PADS.
- 3) ROUNDED PCB LAND PADS REDUCE SOLDER BRIDGING. PAD CHAMFER ANGLE MAY VARY.
- 4) PCB LANDS SHOULD BE 0.2mm LONGER THAN THE PACKAGE I/O PADS.
- 5) THE WIDTH OF PERIMETER PCB PADS SHOULD MATCH (1:1) THE WIDTH OF THE PACKAGE PADS.
- 6) REFER TO INDUSTRY REFERENCES SUCH AS IPC-SM-782 FOR PCB LAND PATTERN DESIGN.
- 7) THERMAL GROUND PADS MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
  - A) MAKE COPPER THERMAL PAD AS LARGE AS POSSIBLE.
  - B) DRILL MULTIPLE THERMAL VIAS 0.25~0.33mm DIAMETER USING 0.8~1.2mm PITCH GRID.
  - C) PLATE THERMAL VIA BARRELS WITH 1-OUNCE COPPER (18µm).
  - D) TENT (COVER) THERMAL VIAS WITH SOLDER MASK 0.1mm LARGER THAN THE VIA DIAMETER.
- 8) STENCIL DESIGN MAY BE CHANGED TO SUIT REQUIREMENTS OF THE DESIGNER.
  - A) LASER CUT STENCIL 0.125mm (5mil) THICK. APERTURE SIZE-TO-LAND RATIO OF 1:1.
  - B) THE SOLDER PASTE OPENING IN THE THERMAL PAD AREA SHOULD BE A MATRIX ARRAY OF SMALLER APERTURES INSTEAD OF ONE LARGE APERTURE TO CONTROL PASTE AMOUNTS.
  - C) APPLY 50% TO 80% SOLDER PASTE COVERAGE IN THE PAD AREA.

<b>Mirror</b> Semiconductor™			
TITLE C-QFN 32L 5x5 P.5mm CERAMIC CAVITY PACKAGE			
SCALE	SIZE	DRAWING NO.	REV
18:1	A	353230	A
DO NOT SCALE DRAWING			SHEET 6 OF 6