20-LEAD 5mm P=0.80mm
QFN CAVITY PACKAGE

Notes: (Unless Otherwise Specified)
1) BODY: PLASTIC, SEMICONDUCTOR GRADE
2) LEAD FRAME: COPPER, C-194F/H
3) LEAD FRAME PLATING: Ni, Pd, Au
4) FRAME THICKNESS: 0.203mm
5) DIE PAD: 3.40 X 3.40mm
6) JEDEC OUTLINE: MO-220

TOLERANCES UNLESS NOTED
X.X ± 0.05
X.XX ± 0.01
X.XXX ± 0.005
X.XXXX ± 0.0005

ALL DIMENSIONS IN
INCHES
MILLIMETERS

THIRD ANGLE PROJECTION

REVISED

DO NOT SCALE DRAWING

DO NOT SCALE DRAWING

Scale: 14:1
Size: A
DWG. NO.: 482070
REV: A

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Mirror Semiconductor
20-LEAD 5mm P=0.80mm
QFN CAVITY PACKAGE
LEAD NUMBERING

CAVITY WALL

45° CHAMFER

0.80 TYP.
Notes: (Unless Otherwise Specified).

1. DIMENSIONS ARE PRESENTED ONLY AS A GUIDELINE. DESIGNERS SHOULD USE THEIR OWN KNOWLEDGE BASE WHEN DESIGNING THE PCB.

2. SURROUND EACH SIDE OF I/O PERIMETER PADS WITH 0.060~0.075 mm (2.4~3.0mils) NSMD SOLDER MASK OPENING. OPTIONALLY OK TO USE RECTANGLE (NSMD) MASK OPENING AROUND I/O PADS.

3. ROUNDED PCB LAND PADS REDUCE SOLDER BRIDGING. PAD CHAMFER ANGLE MAY VARY.

4. PCB LANDS SHOULD BE 0.2mm LONGER THAN THE PACKAGE I/O PADS.

5. THE WIDTH OF PERIMETER PCB PADS SHOULD MATCH (1:1) THE WIDTH OF THE PACKAGE PADS.

6. REFER TO INDUSTRY REFERENCES SUCH AS IPC-SM-782 FOR PCB LAND PATTERN DESIGN.

7. THERMAL GROUND PADS MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
   A. MAKE COPPER THERMAL PAD AS LARGE AS POSSIBLE.
   B. DRILL MULTIPLE THERMAL VIAS 0.25~0.33mm DIAMETER USING 0.8~1.2mm PITCH GRID.
   C. PLATE THERMAL VIA BARRELS WITH 1-OUNCE COPPER (18µm).
   D. TENT (COVER) THERMAL VIAS WITH SOLDER MASK 0.1mm LARGER THAN THE VIA DIAMETER.

8. STENCIL DESIGN MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
   A. LASER CUT STENCIL 0.125mm (5mil) THICK. APERTURE SIZE-TO-LAND RATIO OF 1:1.
   B. THE SOLDER PASTE OPENING IN THE THERMAL PAD AREA SHOULD BE A MATRIX ARRAY OF SMALLER APERTURES INSTEAD OF ONE LARGE APERTURE TO CONTROL PASTE AMOUNTS.
   C. APPLY 50% TO 80% SOLDER PASTE COVERAGE IN THE PAD AREA.