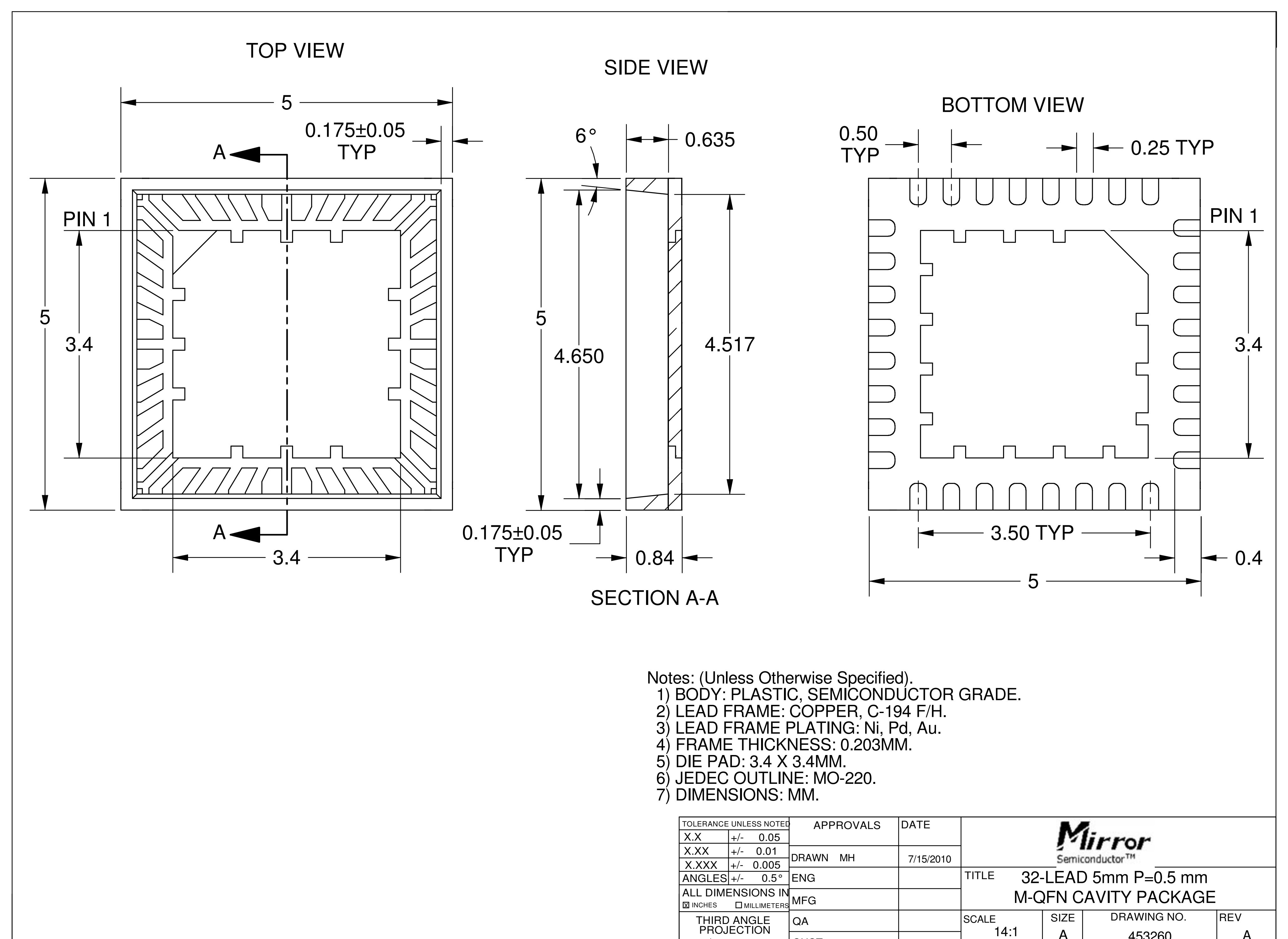

TOP VIEW
SIDE VIEW
BOTTOM VIEW
5
0.175±0.05
TYP
A
PIN 1
5
3.4
A
3.4
6°
0.635
5
4.650
4.517
0.175±0.05
TYP
0.84
SECTION A-A
0.50
TYP
0.25 TYP
PIN 1
3.4
3.50 TYP
0.4
5
Notes: (Unless Otherwise Specified).
1) BODY: PLASTIC, SEMICONDUCTOR GRADE.
2) LEAD FRAME: COPPER, C-194 F/H.
3) LEAD FRAME PLATING: Ni, Pd, Au.
4) FRAME THICKNESS: 0.203MM.
5) DIE PAD: 3.4 X 3.4MM.
6) JEDEC OUTLINE: MO-220.
7) DIMENSIONS: MM.
TOLERANCE UNLESS NOTED
X.X +/- 0.05
X.XX +/- 0.01
X.XXX +/- 0.005
ANGLES +/- 0.5°
ALL DIMENSIONS IN
INCHES
MILLIMETERS
THIRD ANGLE PROJECTION
APPROVALS
DATE
DRAWN MH
7/15/2010
ENG
MFG
QA
CUST
REVISED
Mirror
Semiconductor™
TITLE
32-LEAD 5mm P=0.5 mm
M-QFN CAVITY PACKAGE
SCALE
14:1
SIZE
A
DRAWING NO.
453260
REV
A
DO NOT SCALE DRAWING
SHEET 1 OF 4

PIN LOCATIONS

TOP VIEW

45° CHAMFER

32 31 30 29 28 27 26 25

1 2 3 4 5 6 7 8

24 23 22 21 20 19 18 17

9 10 11 12 13 14 15 16

CAVITY WALL

SIDE VIEW (BEFORE LID ATTACH)

0.84

BOTTOM VIEW

45° CHAMFER

25 26 27 28 29 30 31 32

24 23 22 21 20 19 18 17

1 2 3 4 5 6 7 8

16 15 14 13 12 11 10 9

5

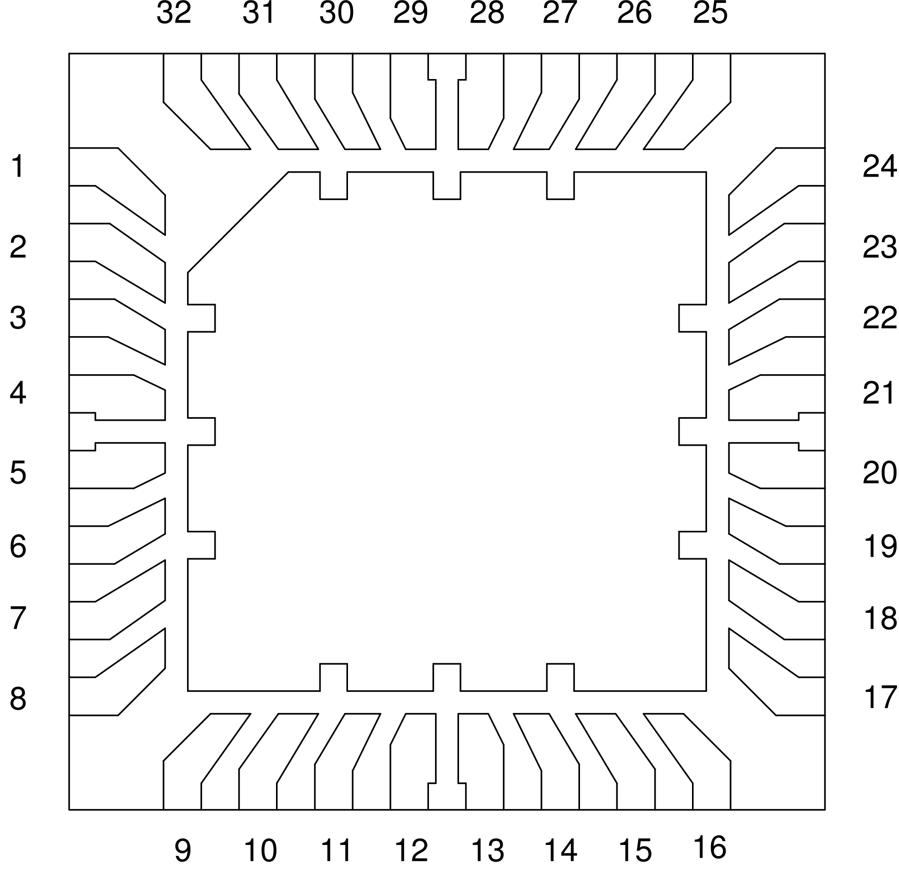
0.50 TYP

5

Mirror Semiconductor™

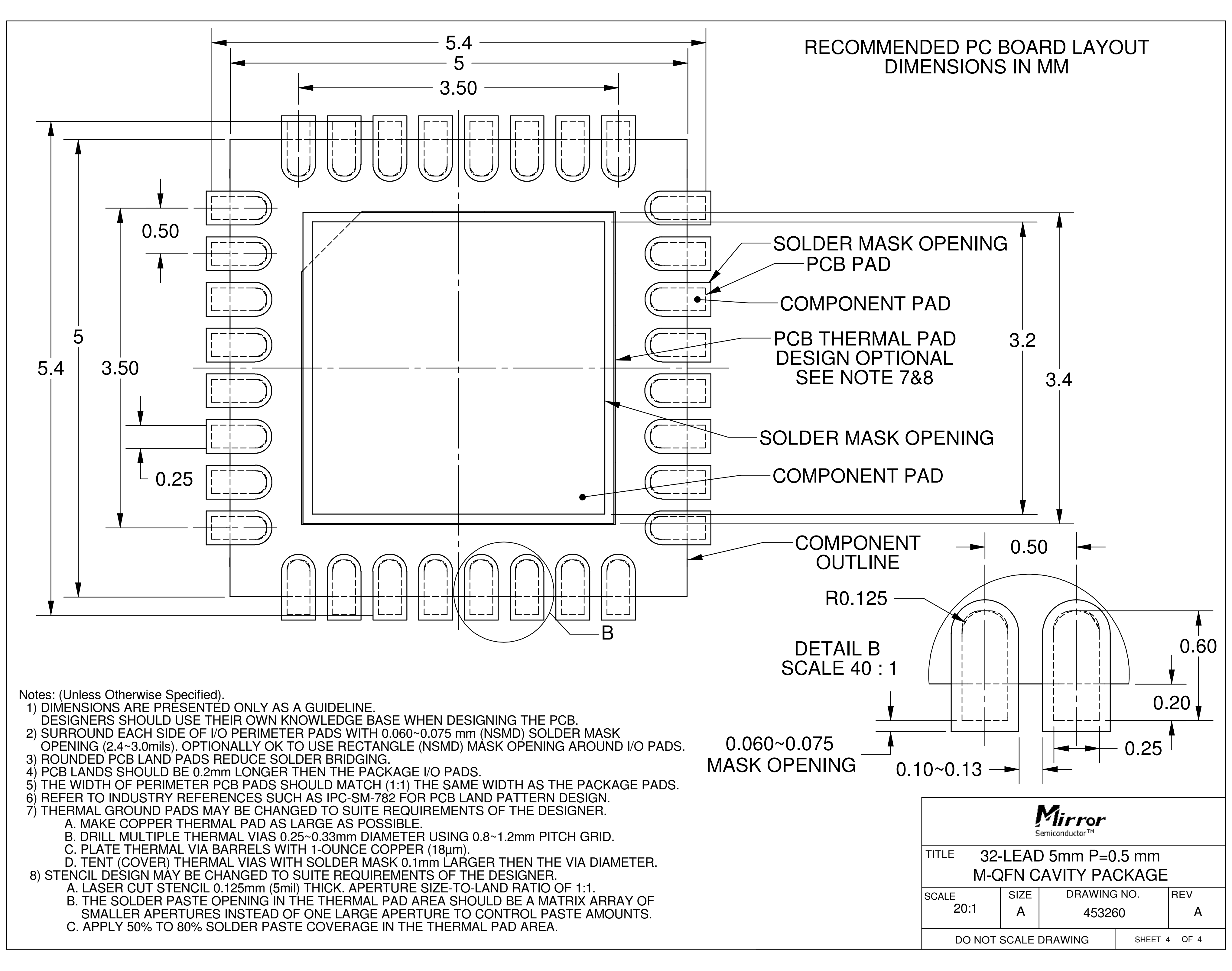
TITLE	32-LEAD 5mm P=0.5 mm M-QFN CAVITY PACKAGE		
SCALE 14:1	SIZE A	DRAWING NO. 453260	REV A
DO NOT SCALE DRAWING		SHEET 2 OF 4	

BONDING DIAGRAM



Mirror Semiconductor™

TITLE	32-LEAD 5mm P=0.5 mm M-QFN CAVITY PACKAGE		
SCALE 20:1	SIZE A	DRAWING NO. 453260	REV A
DO NOT SCALE DRAWING		SHEET 3 OF 4	


RECOMMENDED PC BOARD LAYOUT
DIMENSIONS IN MM
5.4
5
3.50
0.50
5
5.4
3.50
0.25
SOLDER MASK OPENING
PCB PAD
COMPONENT PAD
PCB THERMAL PAD
DESIGN OPTIONAL
SEE NOTE 7&8
3.2
3.4
SOLDER MASK OPENING
COMPONENT PAD
COMPONENT
OUTLINE
B
0.50
R0.125
DETAIL B
SCALE 40 : 1
0.60
0.20
0.060~0.075
MASK OPENING
0.25
0.10~0.13
Notes: (Unless Otherwise Specified).
1) DIMENSIONS ARE PRESENTED ONLY AS A GUIDELINE.
DESIGNERS SHOULD USE THEIR OWN KNOWLEDGE BASE WHEN DESIGNING THE PCB.
2) SURROUND EACH SIDE OF I/O PERIMETER PADS WITH 0.060~0.075 mm (NSMD) SOLDER MASK
OPENING (2.4~3.0mils). OPTIONALLY OK TO USE RECTANGLE (NSMD) MASK OPENING AROUND I/O PADS.
3) ROUNDED PCB LAND PADS REDUCE SOLDER BRIDGING.
4) PCB LANDS SHOULD BE 0.2mm LONGER THEN THE PACKAGE I/O PADS.
5) THE WIDTH OF PERIMETER PCB PADS SHOULD MATCH (1:1) THE SAME WIDTH AS THE PACKAGE PADS.
6) REFER TO INDUSTRY REFERENCES SUCH AS IPC-SM-782 FOR PCB LAND PATTERN DESIGN.
7) THERMAL GROUND PADS MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
A. MAKE COPPER THERMAL PAD AS LARGE AS POSSIBLE.
B. DRILL MULTIPLE THERMAL VIAS 0.25~0.33mm DIAMETER USING 0.8~1.2mm PITCH GRID.
C. PLATE THERMAL VIA BARRELS WITH 1-OUNCE COPPER (18µm).
D. TENT (COVER) THERMAL VIAS WITH SOLDER MASK 0.1mm LARGER THEN THE VIA DIAMETER.
8) STENCIL DESIGN MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
A. LASER CUT STENCIL 0.125mm (5mil) THICK. APERTURE SIZE-TO-LAND RATIO OF 1:1.
B. THE SOLDER PASTE OPENING IN THE THERMAL PAD AREA SHOULD BE A MATRIX ARRAY OF
SMALLER APERTURES INSTEAD OF ONE LARGE APERTURE TO CONTROL PASTE AMOUNTS.
C. APPLY 50% TO 80% SOLDER PASTE COVERAGE IN THE THERMAL PAD AREA.
Mirror
Semiconductor™
TITLE
32-LEAD 5mm P=0.5 mm
M-QFN CAVITY PACKAGE
SCALE
20:1
SIZE
A
DRAWING NO.
453260
REV
A
DO NOT SCALE DRAWING
SHEET 4 OF 4