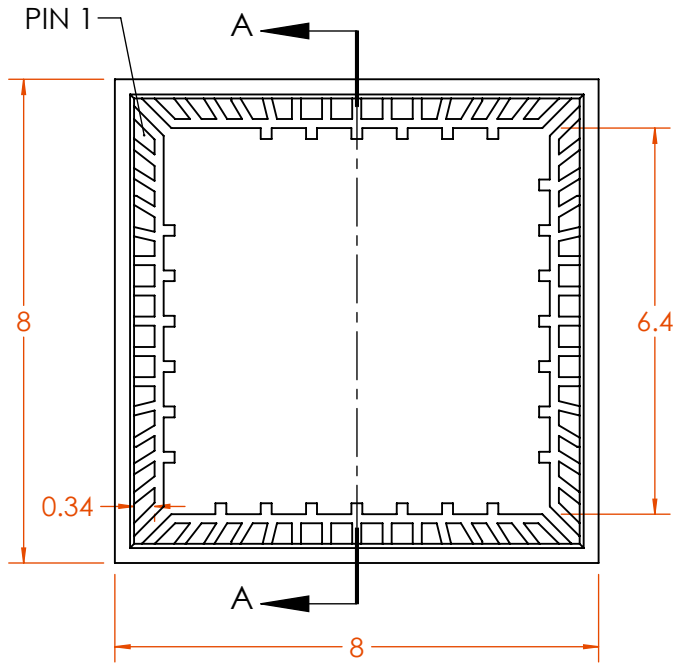
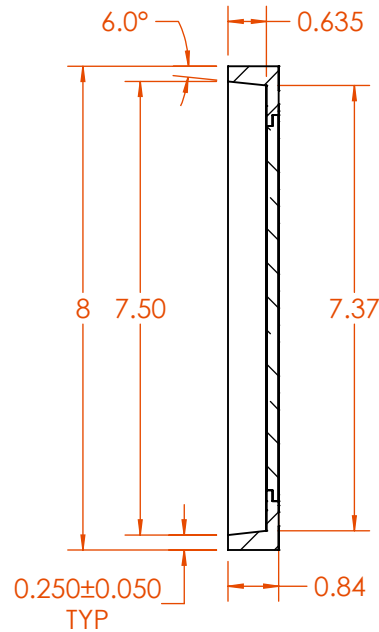


TOP VIEW

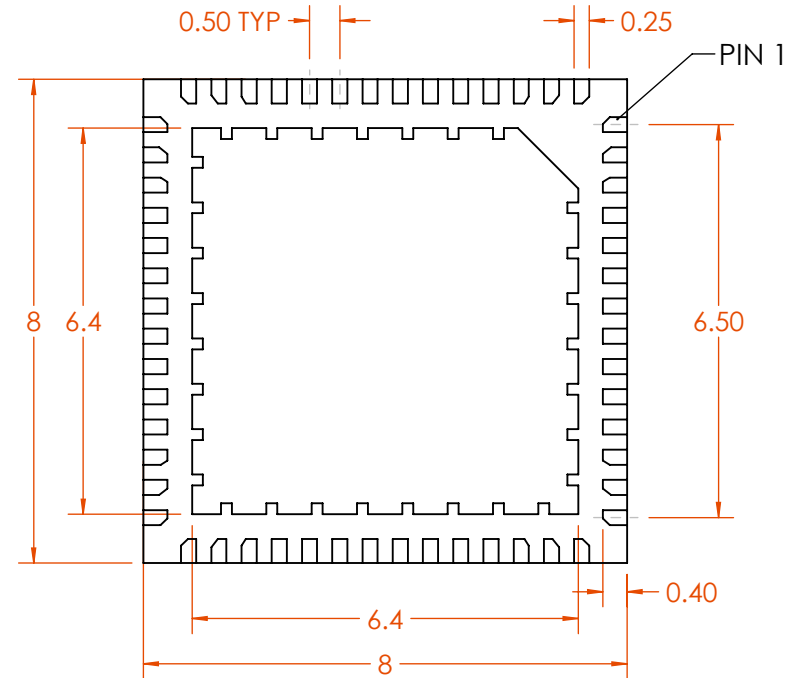


SIDE VIEW

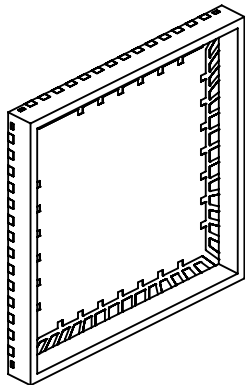


SECTION A-A

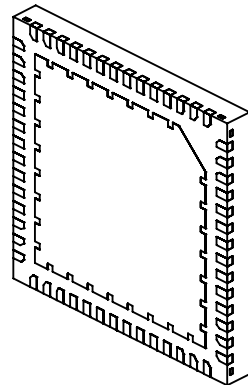
BOTTOM VIEW




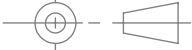
- Notes: (Unless Otherwise Specified)
- 1) BODY; PLASTIC, SEMICONDUCTOR GRADE
  - 2) LEAD FRAME: COPPER, C-194F/H
  - 3) LEAD FRAME PLATING: Ni, Pd, Au
  - 4) FRAME THICKNESS: 0.203mm
  - 5) DIE PAD: 6.4 X 6.4mm
  - 6) JEDEC OUTLINE: MO-220



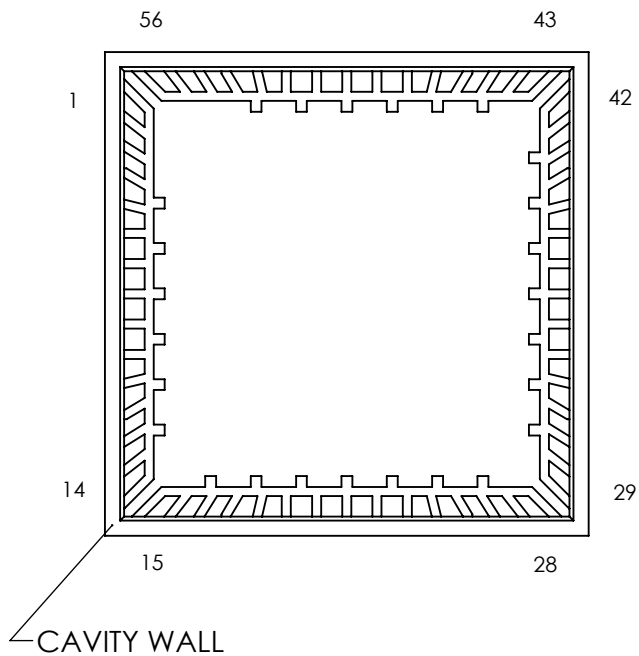
ISOMETRIC VIEW OF CAVITY SIDE



ISOMETRIC VIEW OF PCB SIDE

TOLERANCES UNLESS NOTED		APPROVALS	DATE	 www.MirrorSemi.com								
X.X	± 0.05	DRAWN JMG	05/29/13									
X.XX	± 0.01	CHECKED										
X.XXX	± 0.005	ENG APPR.										
X.XXXX	± 0.0005	MFG APPR.										
ALL DIMENSIONS IN		Q.A.		TITLE: <b>56-LEAD 8mm P=0.50mm QFN CAVITY PACKAGE</b>								
<input type="checkbox"/> INCHES <input checked="" type="checkbox"/> MILLIMETERS		CUST.										
THIRD ANGLE PROJECTION 		REVISED		<table border="1"> <tr> <td>SCALE</td> <td>SIZE</td> <td>DWG. NO.</td> <td>REV</td> </tr> <tr> <td><b>8:1</b></td> <td><b>A</b></td> <td>455670 M-QFN56W.5-G7</td> <td><b>A</b></td> </tr> </table>	SCALE	SIZE	DWG. NO.	REV	<b>8:1</b>	<b>A</b>	455670 M-QFN56W.5-G7	<b>A</b>
SCALE	SIZE	DWG. NO.	REV									
<b>8:1</b>	<b>A</b>	455670 M-QFN56W.5-G7	<b>A</b>									

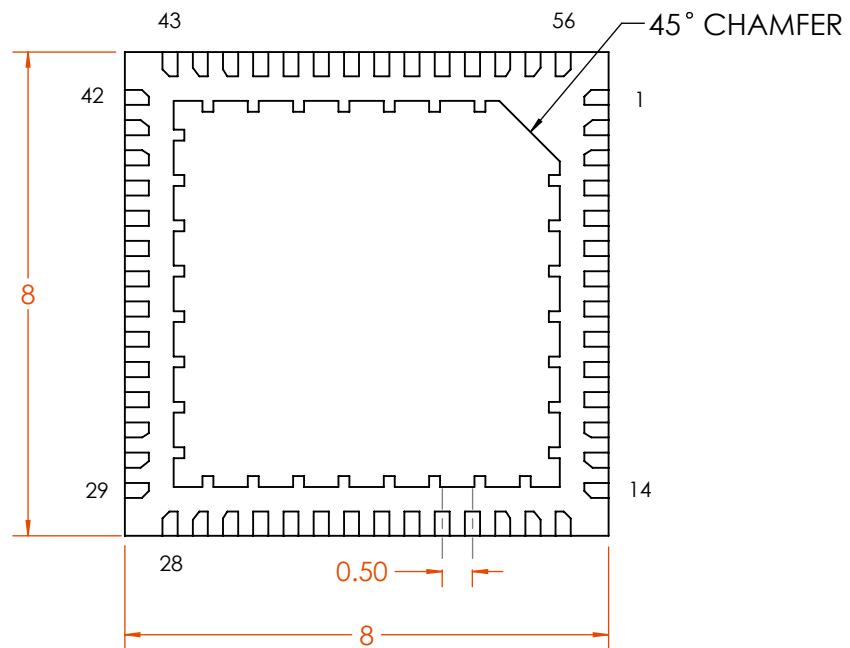
TOP VIEW



SIDE VIEW  
(BEFORE LID ATTACH)



BOTTOM VIEW



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TITLE:

56-LEAD 8mm P=0.50mm  
QFN CAVITY PACKAGE  
LEAD NUMBERING

SCALE

8:1

SIZE

A

DWG. NO.

455670  
M-QFN56W.5-G7

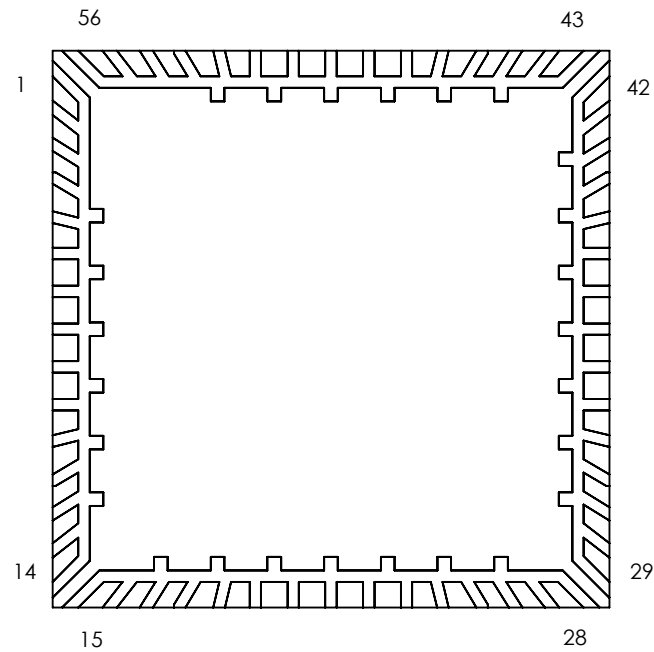
REV

A

DO NOT SCALE DRAWING

SHEET 2 OF 4

# BOND DIAGRAM



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Semiconductor™

[www.MirrorSemi.com](http://www.MirrorSemi.com)

TITLE:

56-LEAD 8mm P=0.50mm  
QFN CAVITY PACKAGE  
BOND DIAGRAM

SCALE

**10:1**

SIZE

**A**

DWG. NO.

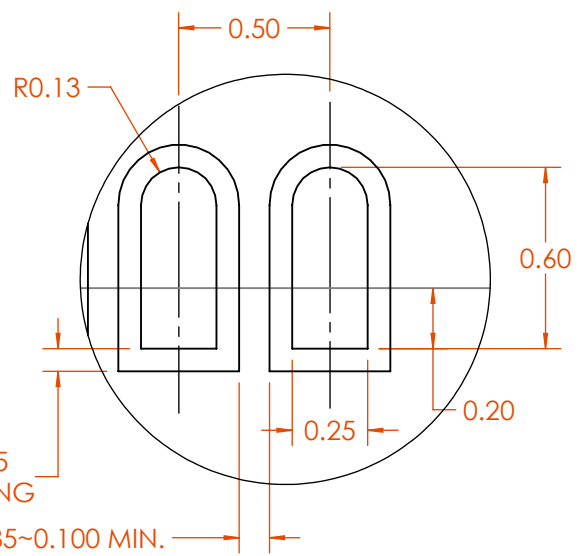
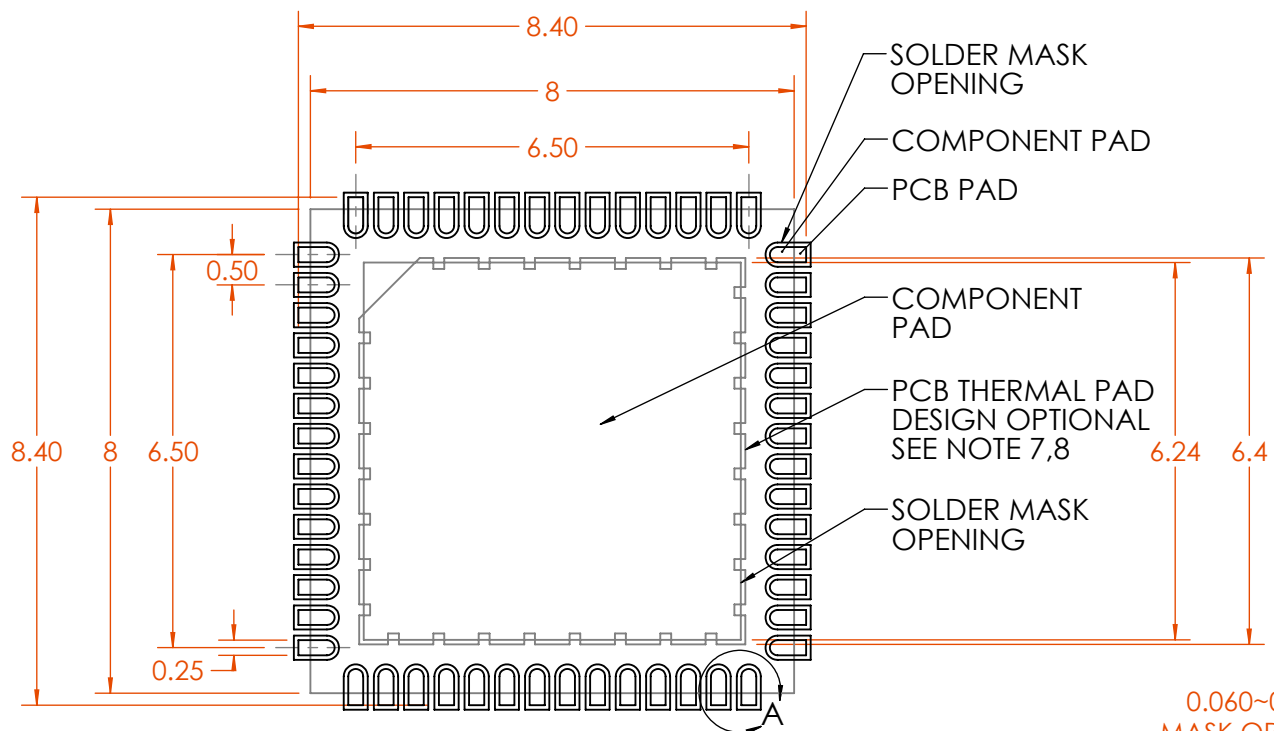
**455670**  
**M-QFN56W.5-G7**

REV

**A**

DO NOT SCALE DRAWING

SHEET 3 OF 4



DETAIL A  
SCALE 40 : 1

Notes: (Unless Otherwise Specified).

1. DIMENSIONS ARE PRESENTED ONLY AS A GUIDELINE. DESIGNERS SHOULD USE THEIR OWN KNOWLEDGE BASE WHEN DESIGNING THE PCB.
2. SURROUND EACH SIDE OF I/O PERIMETER PADS WITH 0.060~0.075 mm (2.4~3.0mils) NSMD SOLDER MASK OPENING. OPTIONALLY OK TO USE RECTANGLE (NSMD) MASK OPENING AROUND I/O PADS.
3. ROUNDED PCB LAND PADS REDUCE SOLDER BRIDGING. PAD CHAMFER ANGLE MAY VARY.
4. PCB LANDS SHOULD BE 0.2mm LONGER THAN THE PACKAGE I/O PADS.
5. THE WIDTH OF PERIMETER PCB PADS SHOULD MATCH (1:1) THE WIDTH OF THE PACKAGE PADS.
6. REFER TO INDUSTRY REFERENCES SUCH AS IPC-SM-782 FOR PCB LAND PATTERN DESIGN.
7. THERMAL GROUND PADS MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
  - A. MAKE COPPER THERMAL PAD AS LARGE AS POSSIBLE.
  - B. DRILL MULTIPLE THERMAL VIAS 0.25~0.33mm DIAMETER USING 0.8~1.2mm PITCH GRID.
  - C. PLATE THERMAL VIA BARRELS WITH 1-OUNCE COPPER (18µm).
  - D. TENT (COVER) THERMAL VIAS WITH SOLDER MASK 0.1mm LARGER THAN THE VIA DIAMETER.
8. STENCIL DESIGN MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
  - A. LASER CUT STENCIL 0.125mm (5mil) THICK. APERTURE SIZE-TO-LAND RATIO OF 1:1.
  - B. THE SOLDER PASTE OPENING IN THE THERMAL PAD AREA SHOULD BE A MATRIX ARRAY OF SMALLER APERTURES INSTEAD OF ONE LARGE APERTURE TO CONTROL PASTE AMOUNTS.
  - C. APPLY 50% TO 80% SOLDER PASTE COVERAGE IN THE PAD AREA.

		<a href="http://www.MirrorSemi.com">www.MirrorSemi.com</a>	
<b>TITLE: 56-LEAD 8mm P=0.50mm QFN CAVITY PACKAGE RECOMMENDED PCB LAYOUT</b>			
SCALE	SIZE	DWG. NO.	REV
<b>8:1</b>	<b>A</b>	455670 M-QFN56W.5-G7	<b>A</b>
DO NOT SCALE DRAWING			SHEET 4 OF 4