TOP

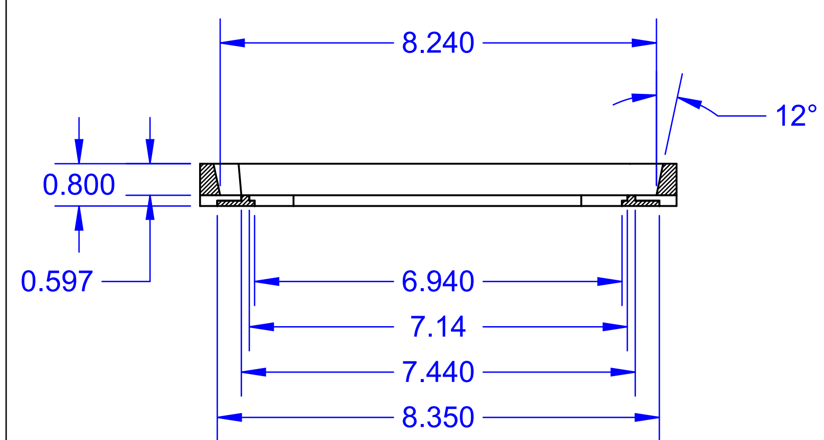
9.000
4.500
PIN #1 ID
0.400 X 45°
CHAMFER
3X R0.500
A
A
7.14
8.494
0.150
0.400
0.150
0.550

SIDE

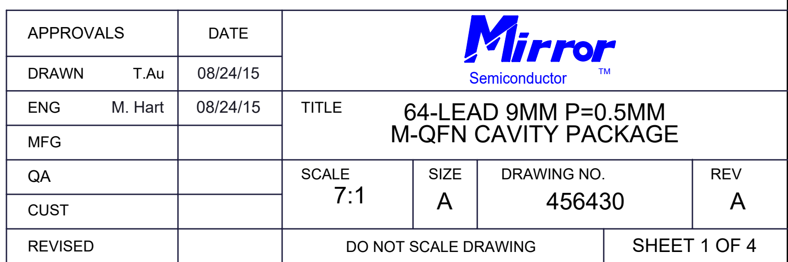
0.203
9.000
0.800

BOTTOM

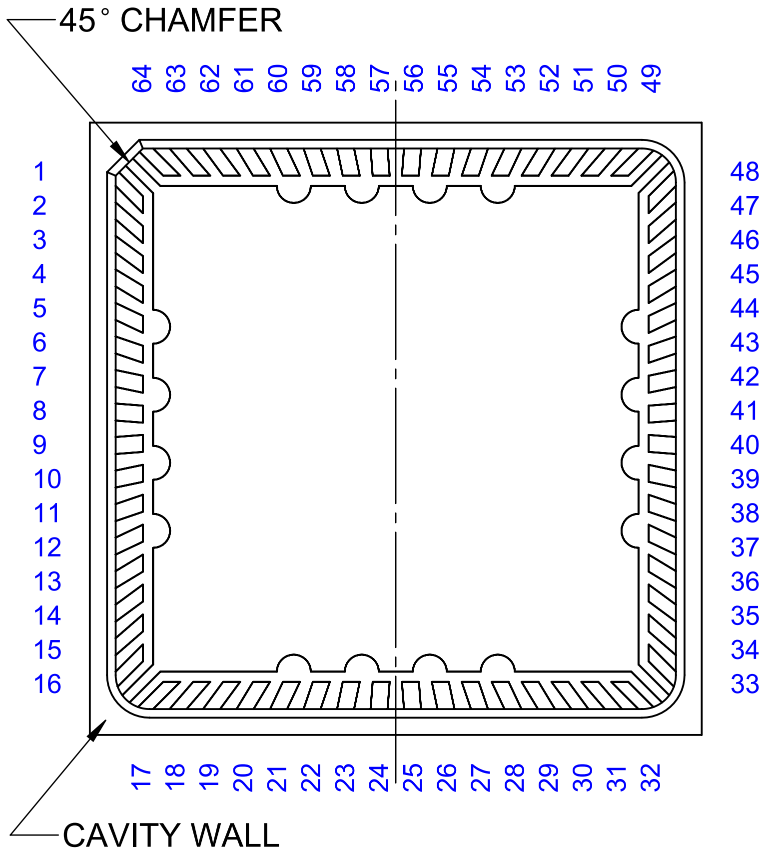
7.500
PIN #1
6.94
9.000
0.250
0.500
0.325

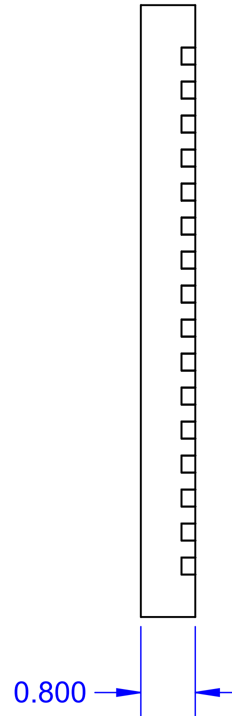


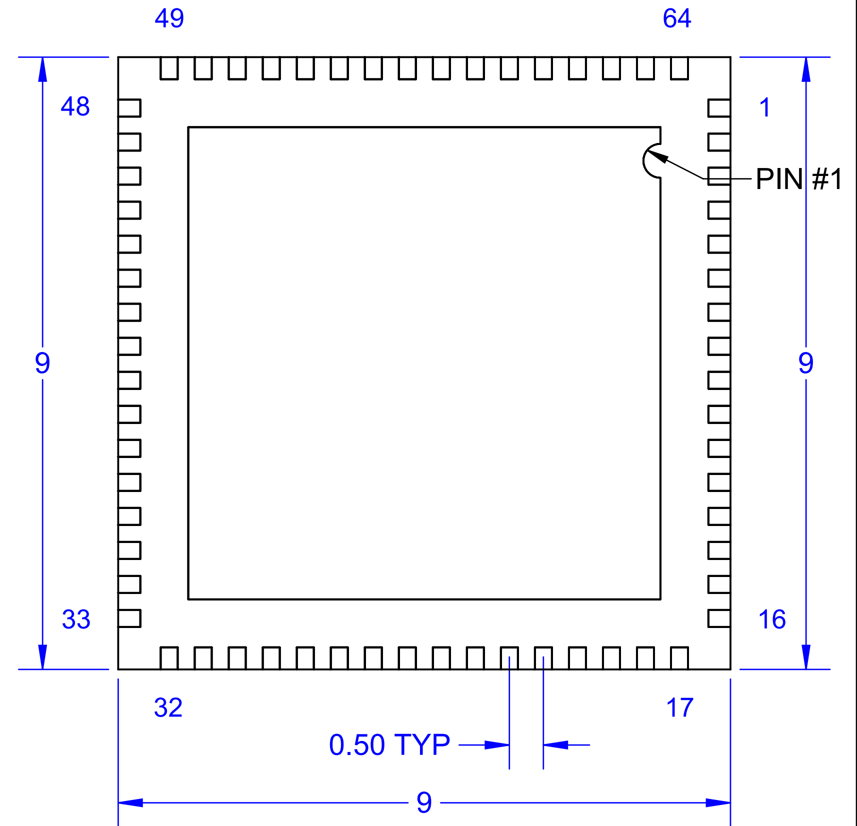
Notes:
1) BODY: PLASTIC, SEMICONDUCTOR GRADE.
2) LEAD FRAME: COPPER C-194FH 0.203µm THICK.
3) LEAD FRAME PLATING: Ni/Au (PART No. SUFFIX - G3).
NICKEL 100~300 MICRO-INCH (2.5µm~7.6µm) THICK.
GOLD 40~80 MICRO-INCH (1µm~2µm) THINCK.
4) DIE PAD: 7.14mm x 7.14mm.
7) DIMENSIONS: MM.

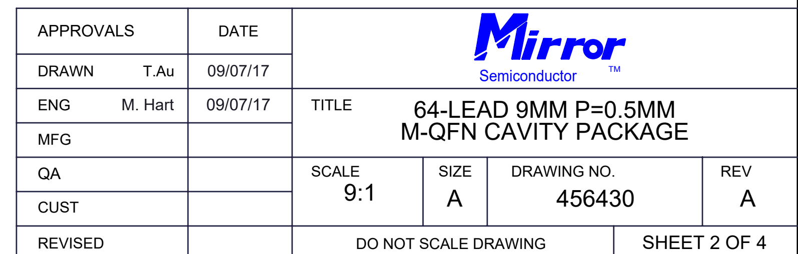


APPROVALS		DATE	Mirror Semiconductor ™			
DRAWN	T.Au	08/24/15				
ENG	M. Hart	08/24/15	TITLE	64-LEAD 9MM P=0.5MM M-QFN CAVITY PACKAGE		
MFG						
QA			SCALE 7:1	SIZE A	DRAWING NO. 456430	REV A
CUST						
REVISED			DO NOT SCALE DRAWING		SHEET 1 OF 4	





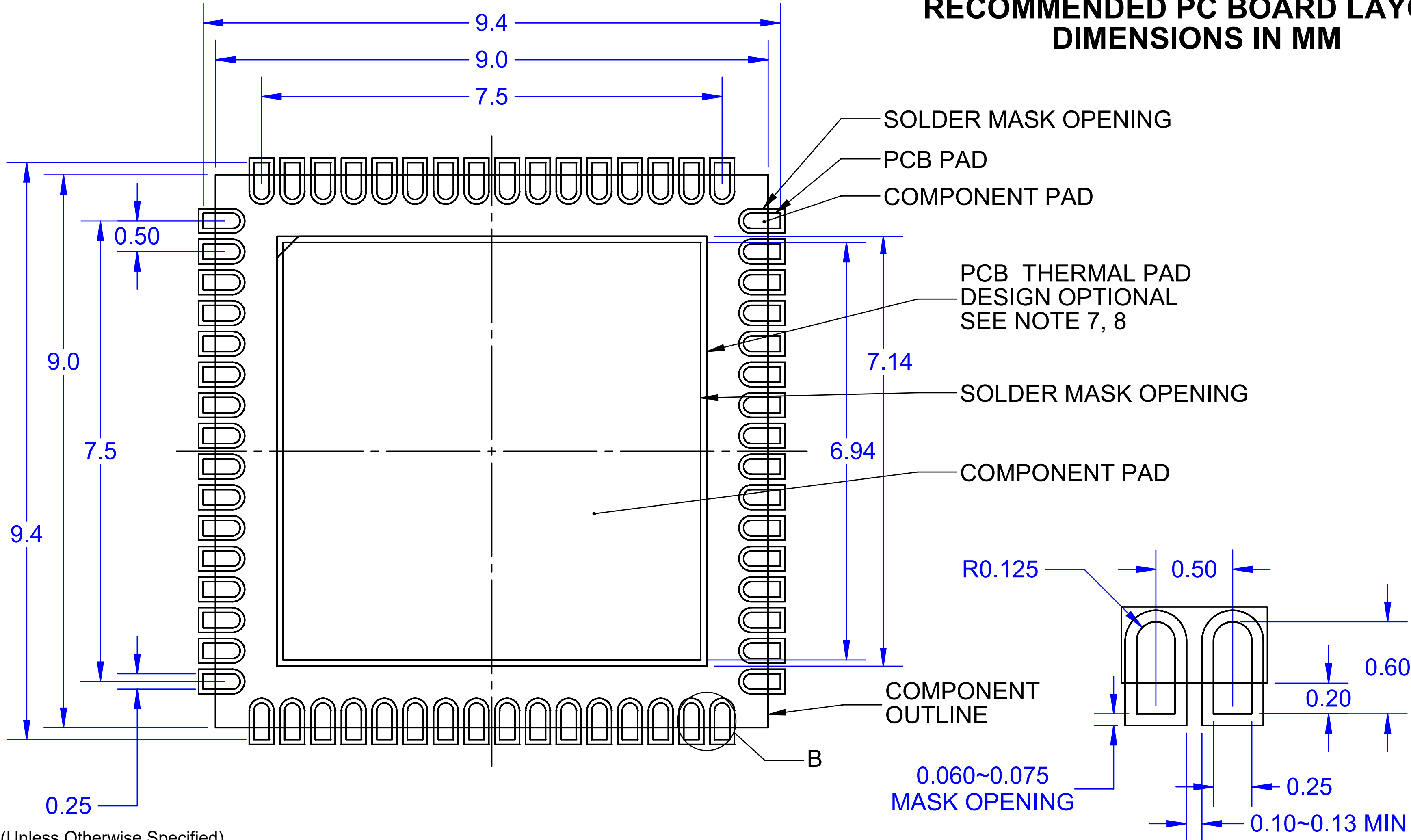




APPROVALS		DATE	
DRAWN	T.Au	09/07/17	Mirror Semiconductor ™
ENG	M. Hart	09/07/17	TITLE 64-LEAD 9MM P=0.5MM M-QFN CAVITY PACKAGE
MFG			
QA			SCALE 9:1 · SIZE A · DRAWING NO. 456430 · REV A
CUST			
REVISED			DO NOT SCALE DRAWING · SHEET 2 OF 4

BOND DIAGRAM

TITLE	64-LEAD 9MM P=0.5MM M-QFN CAVITY PACKAGE		
SCALE 16:1	SIZE A	DRAWING NO. 456430	REV A
DO NOT SCALE DRAWING		SHEET 3 OF 4	



Notes: (Unless Otherwise Specified).

1) DIMENSIONS ARE PRESENTED ONLY AS A GUIDELINE.
   DESIGNERS SHOULD USE THEIR OWN KNOWLEDGE BASE WHEN DESIGNING THE PCB.
2) SURROUND EACH SIDE OF I/O PERIMETER PADS WITH 0.060~0.075 mm (NSMD) SOLDER MASK
   OPENING (2.4~3.0mils). OPTIONALLY OK TO USE RECTANGLE (NSMD) MASK OPENING AROUND I/O PADS.
3) ROUNDED PCB LAND PADS REDUCE SOLDER BRIDGING. PAD CHAMFER ANGLE MAY VARY
4) PCB LANDS SHOULD BE 0.2mm LONGER THAN THE PACKAGE I/O PADS.
5) THE WIDTH OF PERIMETER PCB PADS SHOULD MATCH (1:1) THE SAME WIDTH AS THE PACKAGE PADS.
6) REFER TO INDUSTRY REFERENCES SUCH AS IPC-SM-782 FOR PCB LAND PATTERN DESIGN.
7) THERMAL GROUND PADS MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
   A. MAKE COPPER THERMAL PAD AS LARGE AS POSSIBLE.
   B. DRILL MULTIPLE THERMAL VIAS 0.25~0.33mm DIAMETER USING 0.8~1.2mm PITCH GRID.
   C. PLATE THERMAL VIA BARRELS WITH 1-OUNCE COPPER (18µm).
   D. TENT (COVER) THERMAL VIAS WITH SOLDER MASK 0.1mm LARGER THEN THE VIA DIAMETER.
8) STENCIL DESIGN MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
   A. LASER CUT STENCIL 0.125mm (5mil) THICK. APERTURE SIZE-TO-LAND RATIO OF 1:1.
   B. THE SOLDER PASTE OPENING IN THE THERMAL PAD AREA SHOULD BE A MATRIX ARRAY OF
      SMALLER APERTURES INSTEAD OF ONE LARGE APERTURE TO CONTROL PASTE AMOUNTS.
   C. APPLY 50% TO 80% SOLDER PASTE COVERAGE IN THE THERMAL PAD AREA.

Mirror Semiconductor™

TITLE	64-LEAD 9MM P=0.5MM M-QFN CAVITY PACKAGE		
SCALE 10:1	SIZE A	DRAWING NO. 456430	REV A
DO NOT SCALE DRAWING		SHEET 4 OF 4	