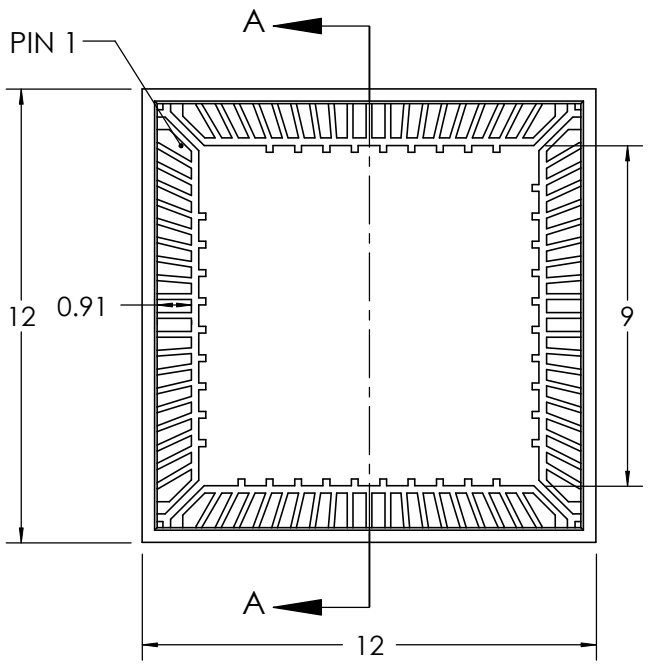
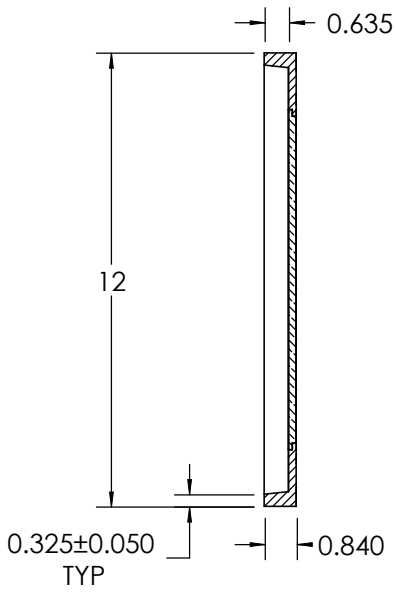
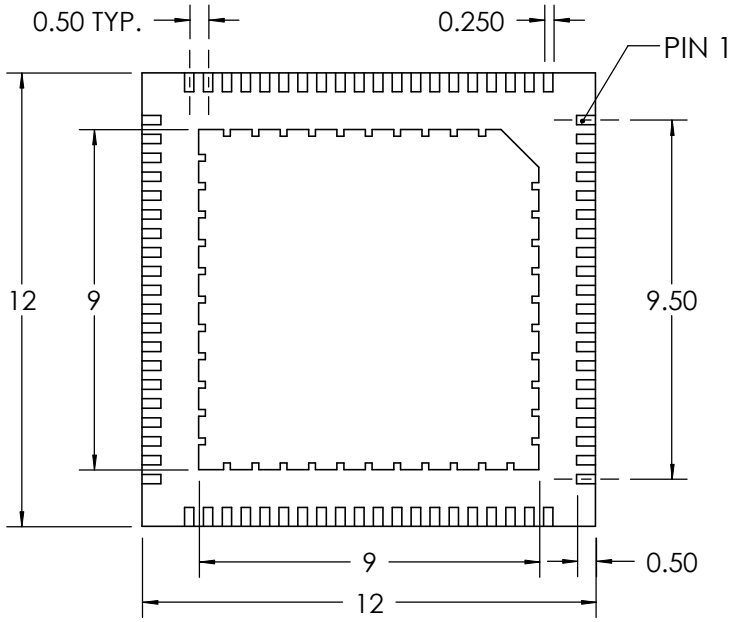
TOP VIEW



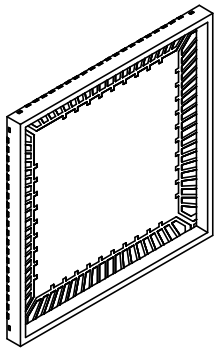
SIDE VIEW



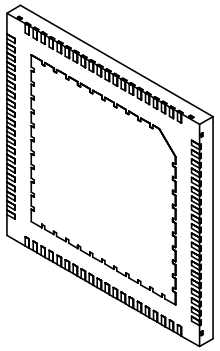
BOTTOM VIEW



SECTION A-A



ISOMETRIC VIEW OF CAVITY SIDE



ISOMETRIC VIEW OF PCB SIDE

Notes: (Unless Otherwise Specified)
1) BODY; PLASTIC, SEMICONDUCTOR GRADE
2) LEAD FRAME: COPPER, C-194F/H
3) LEAD FRAME PLATING: Ni, Pd, Au
4) FRAME THICKNESS: 0.203mm
5) DIE PAD: 9.00 X 9.00mm
6) JEDEC OUTLINE: MO-220

TOLERANCES UNLESS NOTED	
X.X	± 0.05
X.XX	± 0.01
X.XXX	± 0.005
X.XXXX	± 0.0005

ALL DIMENSIONS IN

☐ INCHES ☒ MILLIMETERS

THIRD ANGLE PROJECTION

APPROVALS		DATE
DRAWN	EDK	04/24/2012
CHECKED		
ENG APPR.		
MFG APPR.		
Q.A.		
CUST.		
REVISED		

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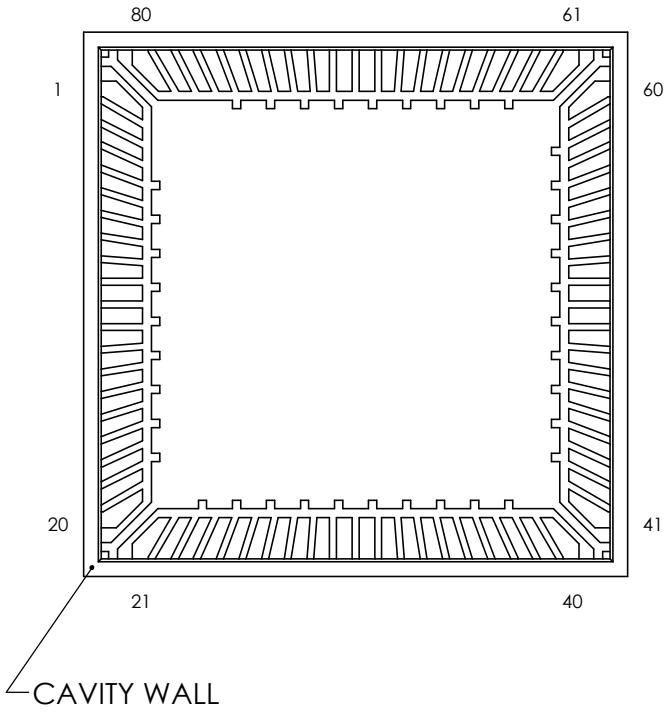
TITLE:

80-LEAD 12mm P=0.50mm QFN CAVITY PACKAGE 0.325mm WALL

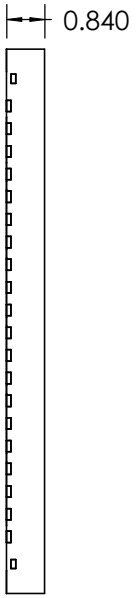
SCALE	SIZE	DWG. NO.	REV
5:1	A	458074 M-QFN80T.5	A

DO NOT SCALE DRAWING | SHEET 1 OF 4

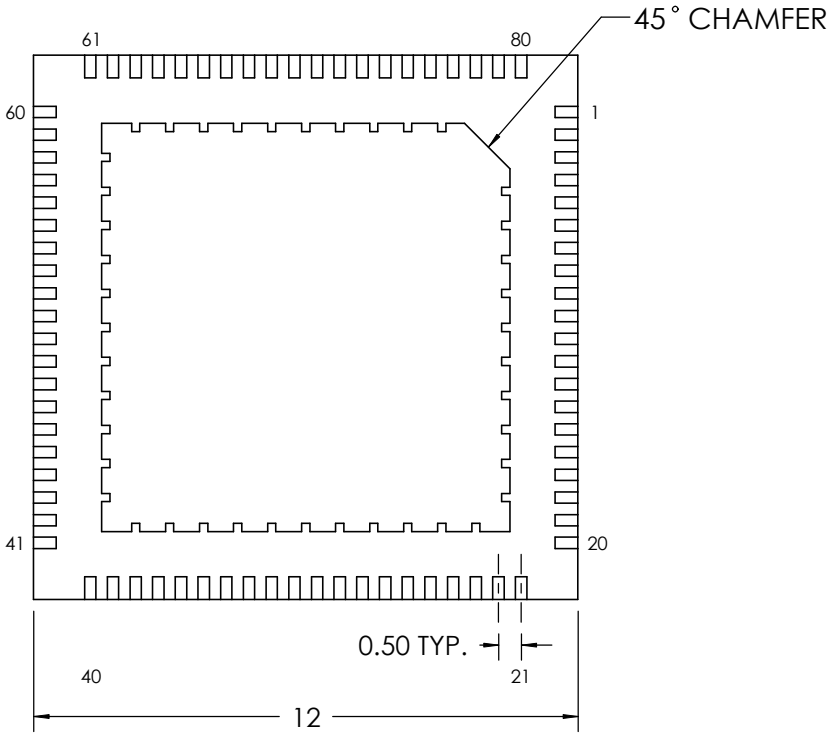
TOP VIEW



SIDE VIEW
(BEFORE LID ATTACH)



BOTTOM VIEW



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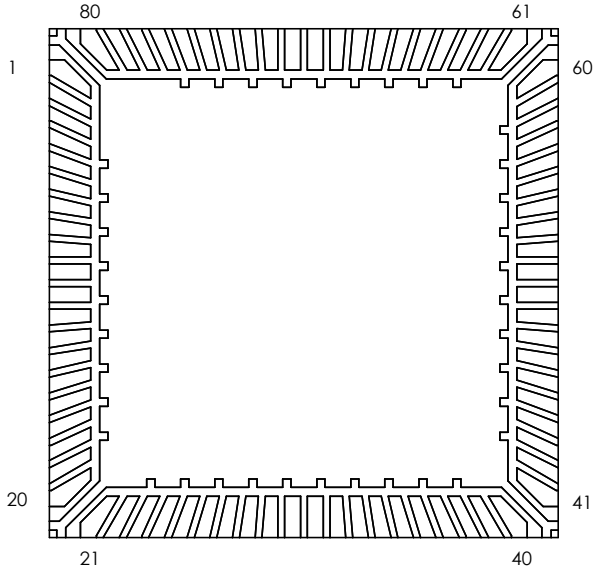
TITLE: 80-LEAD 12mm P=0.50mm
QFN CAVITY PACKAGE
0.325mm WALL
LEAD NUMBERING

SCALE	SIZE	DWG. NO.	REV
6:1	A	458074 M-QFN80T.5	A

DO NOT SCALE DRAWING | SHEET 2 OF 4

BOND DIAGRAM



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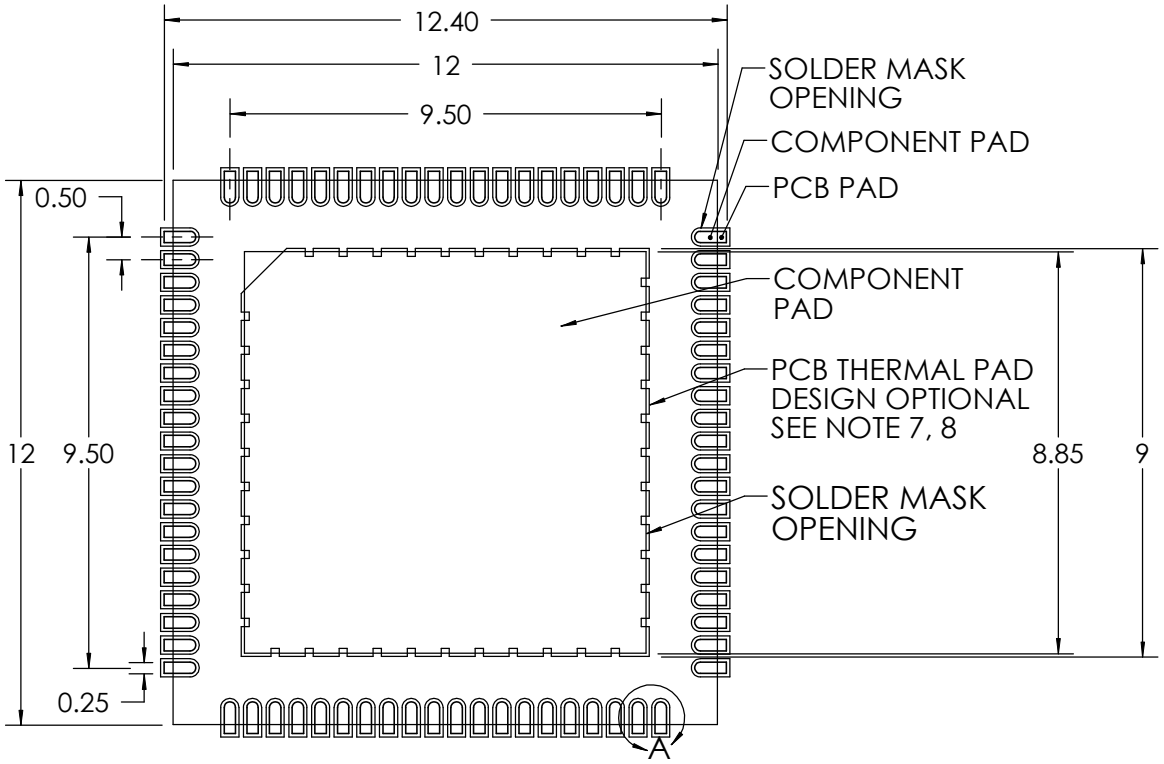
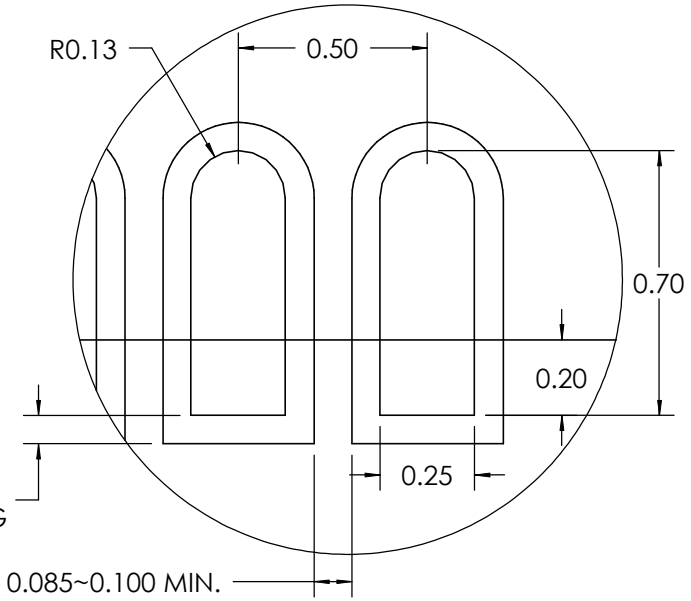
TITLE: 80-LEAD 12mm P=0.50mm QFN CAVITY PACKAGE 0.325mm WALL BOND DIAGRAM			
SCALE **6:1**	SIZE **A**	DWG. NO. **458074 M-QFN80T.5**	REV A
DO NOT SCALE DRAWING		SHEET 3 OF 4	





DETAIL A
SCALE 50 : 1

Notes: (Unless Otherwise Specified).

1. DIMENSIONS ARE PRESENTED ONLY AS A GUIDELINE. DESIGNERS SHOULD USE THEIR OWN KNOWLEDGE BASE WHEN DESIGNING THE PCB.
2. SURROUND EACH SIDE OF I/O PERIMETER PADS WITH 0.060~0.075 mm (2.4~3.0mils) NSMD SOLDER MASK OPENING. OPTIONALLY OK TO USE RECTANGLE (NSMD) MASK OPENING AROUND I/O PADS.
3. ROUNDED PCB LAND PADS REDUCE SOLDER BRIDGING. PAD CHAMFER ANGLE MAY VARY.
4. PCB LANDS SHOULD BE 0.2mm LONGER THAN THE PACKAGE I/O PADS.
5. THE WIDTH OF PERIMETER PCB PADS SHOULD MATCH (1:1) THE WIDTH OF THE PACKAGE PADS.
6. REFER TO INDUSTRY REFERENCES SUCH AS IPC-SM-782 FOR PCB LAND PATTERN DESIGN.
7. THERMAL GROUND PADS MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
   - A. MAKE COPPER THERMAL PAD AS LARGE AS POSSIBLE.
   - B. DRILL MULTIPLE THERMAL VIAS 0.25~0.33mm DIAMETER USING 0.8~1.2mm PITCH GRID.
   - C. PLATE THERMAL VIA BARRELS WITH 1-OUNCE COPPER (18µm).
   - D. TENT (COVER) THERMAL VIAS WITH SOLDER MASK 0.1mm LARGER THAN THE VIA DIAMETER.
8. STENCIL DESIGN MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
   - A. LASER CUT STENCIL 0.125mm (5mil) THICK. APERTURE SIZE-TO-LAND RATIO OF 1:1.
   - B. THE SOLDER PASTE OPENING IN THE THERMAL PAD AREA SHOULD BE A MATRIX ARRAY OF SMALLER APERATURES INSTEAD OF ONE LARGE APERATURE TO CONTROL PASTE AMOUNTS.
   - C. APPLY 50% TO 80% SOLDER PASTE COVERAGE IN THE PAD AREA.

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TITLE: 80-LEAD 12mm P=0.50mm QFN CAVITY PACKAGE 0.325mm WALL RECOMMENDED PCB LAYOUT

SCALE	SIZE	DWG. NO.	REV
6:1	A	458074 M-QFN80T.5	A

DO NOT SCALE DRAWING | SHEET 4 OF 4